Loss Characterization and Modeling of Class II Multilayer Ceramic Capacitors: A Synergic Material-Microstructure-Device Approach

Yunlei Jiang, *Member, IEEE,* Borong Hu, *Member, IEEE,* Yanfeng Shen, *Member, IEEE,* Xufu Ren, *Student Member, IEEE,* Steve Sandler, *Member, IEEE,* Stephan Hofmann, and Teng Long, *Member, IEEE*

***Abstract*—This paper motivates the loss characterization and modeling of Class II multi-layer ceramic capacitors (MLCCs), which have been widely utilized owing to high energy density, in high-frequency resonant converters. In a resonant tank, MLCCs experience complex electrical operating conditions (e.g., large-signal, high-frequency, DC bias), but the incurred power loss has not been clearly characterized and modeled. This paper first proposes a novel resonant-Sawyer-Tower (Res-ST) circuit which can experimentally extracts the loss of a MLCC in real operation in a resonant tank. A general loss modeling approach named Steinmetzs Pre-electrified Graph (SPeG) is then proposed to correlate capacitor's loss to the peak value of excitation, frequency, and DC bias voltage. The SpeG model provides the material-specific volume loss density of common Class II dielectric materials and can be easily extrapolated to evaluate the loss of the MLCCs with different rated voltage&capacitance but employing the same dielectric material. To generalize the material-specific SPeG model to device-level application, this paper also proposes an easy-to-follow tool, dielectric thickness observer (DTO), to estimate the internal microstructural geometry by tracking the C-V characteristic provided in product datasheet. The synergy of the proposed characterization circuit, SPeG loss model, and DTO establishes a toolkit that enables the estimation of MLCC losses in a manner similar to that of a ferromagnetic inductor/transformer core. This paper is accompanied by microscope images of the investigated MLCC samples and MATLAB scripts of the proposed DTO.**

***Index Terms*—Class II, ceramic capacitor, high frequency, resonant converter, ferroelectric material, loss modeling, Steinmetz's equation**

I. Introduction

CAPACITORS play a crucial role as key components in power electronics converters, encompassing applications such as DC-link, filters, and resonant tanks, covering a wide frequency range from tens of Hz to mega-Hz [1]. The multilayer ceramic capacitors (MLCCs) have a compact format of alternatively sintering hundreds of thin layers (a few micrometers each) of metal electrode and ceramic dielectric. As one of the most popular high energy density capacitors, they are particularly favored in volume-sensitive designs. In comparison to Class I counterparts, Class II MLCCs using $BaTiO_3$-based ferroelectric dielectric material with a dielectric constant of 1,000-10,000 have attracted more interest in applications where high power density is pursued.

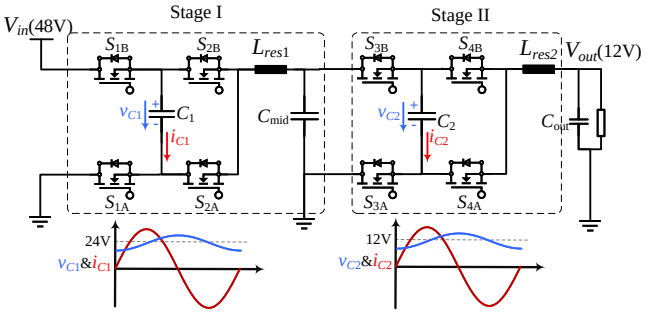


Fig. 1. A representative application where Class II capacitors are used for both resonant and input/output capacitors and are therefore exposed to large-signal, high-frequency excitation superimposed on a bias electric field: 48-12V cascaded resonant switched-capacitor converter.

Class II MLCCs find extensive use in applications such as filter capacitors in AC-tied systems, where they are subjected to high-amplitude excitation at relatively low-frequencies [2], as well as energy transfer elements in resonant switched-capacitor converters (RSCs) [3]. For high-compact RSC applications, which are the primary focus of this work, Class II MLCC can serve as the primary energy transfer device over inductors in a series resonant tank operating at frequencies exceeding 100 kHz [3]–[5], as increasing the capacitance can eliminate physical inductors, resulting in a magnetic-free design [5] [6]. In a typical cascaded RSC, c.f. Fig. 1, for instance, two high-capacitance capacitor banks, i.e. C_1 and C_2, undergo high-frequency and large-signal excitations superimposing 24V and 12V DC bias voltage, respectively. However, the large signal equivalent series resistance (ESR) and power loss of Class II MLCCs under high-frequency and large-amplitude excitations have unfortunately not been adequately investigated.

Under large-signal excitations, due to the ferroelectric hysteresis of $BaTiO_3$-based dielectric materials, Class II ML-

This work was supported by the U.K. Engineering and Physical Sciences Research Council (EPSRC) under Grant EP/T02030X/1; in part by the Jardine Foundation; and in part by the Cambridge Trust. *(Corresponding author: Teng Long, Borong Hu.)*

Yunlei Jiang was with the Electrical Engineering Division, Department of Engineering, University of Cambridge, CB3 0FA Cambridge, U.K, and is now with the Space Exploration Technologies Corporation, Hawthorne, CA 90230, US. (e-mail: yunlei.jiang@spacex.com).

Borong Hu, Xufu Ren, Stephan Hofmann, and Teng Long are with the Electrical Engineering Division, Department of Engineering, University of Cambridge, CB3 0FA Cambridge, U.K. (e-mail: bh529@cam.ac.uk, xr222@cam.ac.uk, tl322@cam.ac.uk).

Yanfeng Shen is with Danfoss Silicon Power R&D Munich, 85737 Ismaning, Germany. (e-mail: ys523@cantab.ac.uk).

Steve Sandler is with the Picotest, Phoenix, AZ, 85085, US. (e-mail: steve@picotest.com).

CCs yield significantly different loss characteristics or ESR compared to the values specified in datasheets, which are extracted from small-signal tests and referenced for low power applications [7]. A universal large-signal loss model of Class II MLCCs is always desired, but an accurate one is difficult to obtain, because of their low dissipation factor and nonlinear electrical hysteresis behavior, under the excitations of large amplitudes and wide-range frequencies.

Although the physics underlying the loss mechanism of Class II MLCCs is not yet fully understood, the nonlinear electrical hysteresis has been identified as the primary source of loss and the underlying cause of the discrepancy between small and large-signal losses [7], [8]. Based on the observation of large-signal charge versus voltage (Q-V) curves, such hysteresis loss has been fitted by Steinmetzs Equation (SE): $P = k_Q f^{\alpha} Q_{pk}^{\beta}$, which relates the peak value of charge Q_{pk}, frequency f and loss P, first giving a quantitative estimation of MLCC's power loss [2], [7]. However, due to the limited frequency covered by conventional testing methods and the lack of interest in high frequency, the frequency dependence of MLCC loss has not been disclosed, resulting in the speculation that frequency exponent α can be approximated to 1 and Q-V loop area is frequency-independent. Additionally, the loss of Class II MLCCs was suspected to be sensitive to DC bias voltage in [9] and [10]. Such sensitivity is dependent on the manufacturers and product series but has not been fully quantified and modeled, due to the absence of an effective experimental characterization methodology. Therefore, in order to unveil the actual loss mechanism and develop a reliable analytical model for Class II MLCC, comprehensive investigations on a wide range of MLCCs involving large-signal measurement, DC voltage bias, and detailed knowledge of the internal microstructure of the MLCCs need to be accordingly conducted.

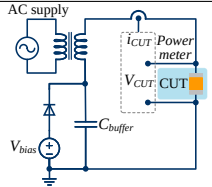
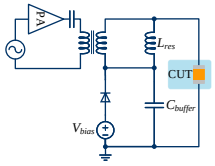
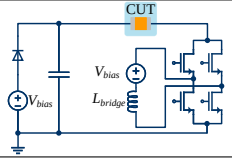
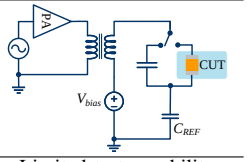
This study intends to synergize characterization approaches using small and large-signal electrical measurements and material-level microscopy investigation for an accurate loss model of Class II MLCCs in RSC-oriented applications. The frequency range of interest spans from several hundred hertz to a hundred kilohertz, encompassing the simultaneous presence of DC voltage bias. The characterization and modeling process pay much attention to elucidating the power loss behavior at the material level. The contributions of the work can be summarized as follows:

1) An experimental loss characterization method for MLCCs under the coexistence of large-signal, wide-range frequency excitations and DC bias is developed based on a novel resonant-Sawyer-Tower (Res-ST) circuit. This method is also applicable to other capacitors under test (CUTs) which are sensitive to the level of excitation, such as anti-ferroelectric CeraLink capacitors;
2) The ferroelectric hysteresis behavior of four dielectric materials has been quantitatively identified with the help of a scanning electron microscope (SEM). The SEM is employed to examine the internal micro-structure of commercial Class II MLCCs to obtain the equivalent plate capacitor model. The microscopic information isolates the influence from MLCCs' nickel electrodes and insulation packaging and enables a material-specific description of loss characteristics;
3) The proposed Steinmetz Pre-electrified Graph (SPeG) enables material-specific loss characterization and models the loss characteristics of dielectric materials. What sets SPeG apart is its ability to incorporate the influence of both DC bias and frequency into the loss modeling, making it the first of its kind to do so;
4) Applying the proposed SPeG on other MLCCs requires the internal microstructural geometry information to be known. A dielectric thickness observer is therefore proposed, which can estimate the geometry information of a MLCC from its electrical characteristics. This method extends the applicability of the material-specific loss model (SPeG) to all the MLCC devices employing the same dielectric material, which provides users with an easy-to-follow power loss estimation route of Class II MLCC.

The manuscript is organized as follows. Section II provides an overview of the state-of-the-art loss characterization methods for Class II MLCCs and outlines the motivation behind this work. Section III details the proposed characterization methodology based on the Res-ST circuit and presents large-signal experimental results from samples with different dielectric materials, e.g. X5R, X7R and X7T. Section IV investigates the loss characterization at a material level, and proposes a method to estimate the geometry of MLCCs based on small-signal measurements, thereby linking material-specific information to device-specific information. Validations of the loss model on a broad range of MLCCs and a 400W 2:1 RSC converter are presented in Section V. Finally, conclusions are drawn in Section VI.

II. Review of Characterization and Modeling of Class II MLCCs

TABLE I
Overview of Q-V loop characterization systems for MLCC

Type	A.Power Meter Measurement [11]	B.PA Resonant Circuit [12]
Structure		
Issues	Limited accuracy	Indirect loss extraction
Type	C.Current-source Measurement [9]	D.ST Circuit [2]
Structure		
Issues	Non-sinusoidal excitation, no Q-V curve	Limited test capability for high-frequency/ capacitance CUTs

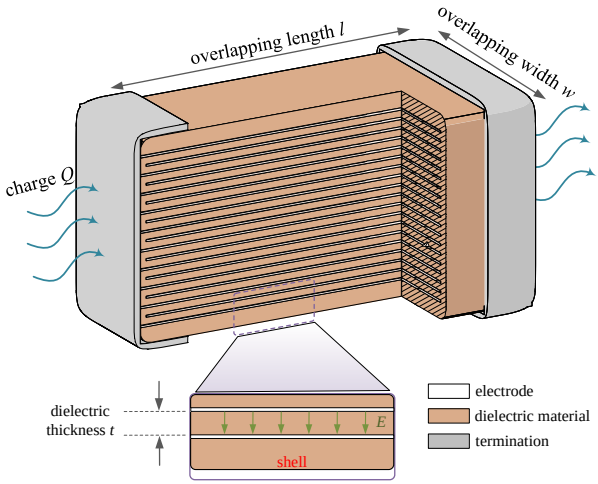


Fig. 2. Cross-section of a typical SMD MLCC overlapping structure: the dielectric material is the main body inside which a large number of overlapped electrode plates are terminated at the two ends of the body for external connections.

A. Excitation Circuits for MLCC Characterization

In previously reported experimental characterizations, difficulties have been identified in terms of circuit designs, excitation sources, power loss separation [11], and operating temperature decoupling. Four typical characterization rigs in the literature following the call for large-signal characterization of Class II MLCCs are summarized in Table I. Using an AC power supply and a transformer as the excitation source, as shown in Type A, is mostly applicable to low excitation frequency measurement [11]. Type B employs a radio-frequency (RF) power amplifier (PA) as the high-frequency excitation source [12], whilst a resonant circuit is constructed to reduce the current requirement from the PA. However, the use of the calorimetry approach for power loss extraction cannot decouple the temperature dependence of ferroelectric dielectric material. In Type C, a current-source excitation circuit consisting of a high-inductance L_{bridge} can excite the CUT with a sawtooth waveform [9], but harmonic components are naturally contained in the excitation. In addition, using a power meter to measure the power loss across the CUT in Type A [11] may compromise accuracy due to low sensitivity. All of these mentioned approaches prove to fit designated applications, where only qualitative characterization is of interest, the test frequency is low, the temperature dependence is negligible, and the exact Q-V curve is not a must.

Among these four approaches, the Sawyer-Tower (ST) circuit has been proven successful to extract the Q-V curve in Type D. This method allows for direct electric charge measurement through the reference capacitor (C_{REF}) by series connecting C_{REF} and CUT, thereby avoiding error-prone current measurements [13]. However, high-power PA can struggle to excite high-capacitance samples at high frequency considering the limitation in PA's current capability. For instance, driving a $10\mu F$ CUT at 100kHz with 10V peak-peak excitation requires a peak excitation current as high as 31A, which by far exceeds the capability of most commercially available PAs. Meanwhile, the reference capacitor C_{REF} is recommended to have a much higher capacitance than that of C_{DUT} in order for C_{DUT} to share more voltage in the series-connected C_{REF}/C_{DUT} voltage divider [2], [14]. This, however, requires a significant number of reference capacitors when high-capacitance CUTs are of interest.

To characterize MLCCs with a wide range of capacitances, it is necessary to develop a more flexible excitation solution that can supply high-power excitations in sinusoidal forms over a wide range of operating frequencies [15]. Furthermore, it is preferable to electrically extract the power losses of MLCCs from the charge-voltage hysteresis loop (Q-V loop), which also indicates the capacitance variation under different excitations. In this work, a resonant Sawyer-Tower (Res-ST) circuit is proposed accordingly to address these aforementioned challenges, as will be stated in Section III.

B. Loss Modeling of Class II MLCCs

The hysteresis behavior of MLCC's charge against voltage (Q-V curve), which shares many similarities with the B-H hysteresis curve of magnetic materials, has been identified as the main source of power loss. Based on this ground, the correlation between peak value of charge (Q_{pk}) and loss (P_{loss}) is then noticed and fitted by Steinmetz's equation to represent the loss of a MLCC under specific charge Q_{pk} and operation frequency f in [2] as:

$$P_{loss} = k_Q \cdot f^{\alpha} \cdot Q_{pk}^{\beta} \tag{1}$$

This modeling approach has proven to be accurate by fitting different sets of loss parameters (α, β, and k_Q) for each MLCC, accommodating their unique loss characteristics. This feature, however, limits the generalization of this charge-based loss model due to the large number of commercially available MLCCs, even from the same manufacturers.

In [8], a new Steinmetz model has been proposed to address this limitation by predicting MLCC loss using a material-specific modeling approach. Fundamentally, this approach makes an assumption that the rated voltage (V_{rated}) of the MLCC is limited by the breakdown voltage of dielectric material. Therefore, the dielectric thickness t between the positive and negative electrode in any layers of a specific type of MLCC, e.g. X5R, X7R, X7T, et al., is expected to be proportional to its rated voltage (V_{rated}) specified by the manufacturer. This assumption then enables the scaling of the measured loss from one benchmark to its peers using the same dielectric material, largely alleviating testing efforts.

This model's prediction error is under 20% when evaluating high-voltage MLCCs [8]. However, it may lose accuracy in lower voltage ranges, after surveying on 31 samples from both high-voltage and low-voltage categories. In Fig. 3, the correlation between dielectric thickness and rated voltage of four types of MLCCs are plotted by inspecting the microstructure of MLCC samples with the aid of SEM, which are detailed in Section V.

As shown in Fig. 3.(a) and (b), the linear scaling claim between the dielectric thickness t and V_{rated} is correct for high-voltage X7T(100V-630V) and X7R(100V-630V) MLCCs. However, such linear correlation no longer holds in

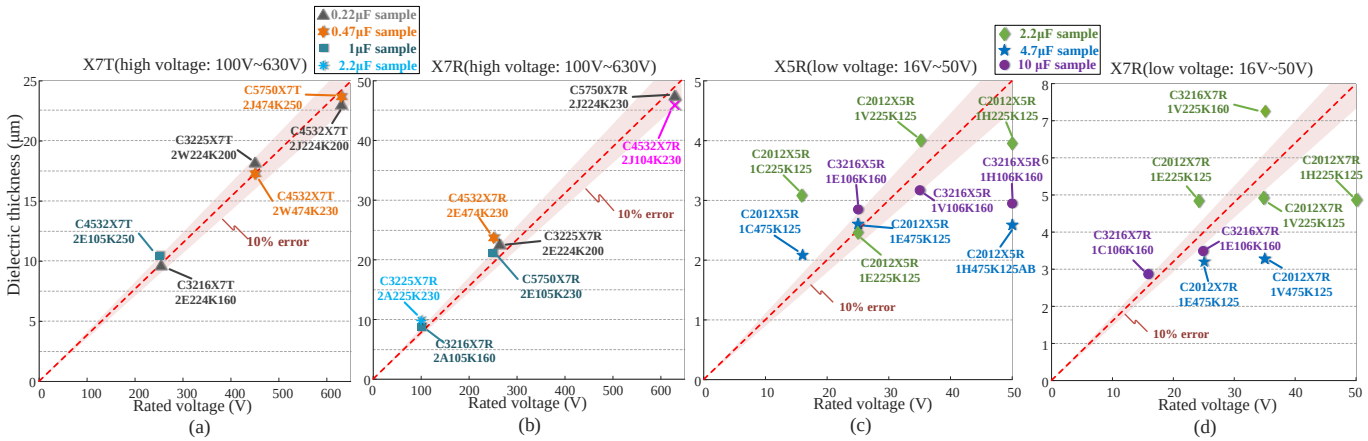


Fig. 3. Correlation between dielectric thickness (t) and rated voltages of four types of MLCCs: high voltage (rated from 100V-630V) MLCCs using X7R and X7T dielectric materials (Fig. 3.(a)&(b)) and low voltage (rated from 16V-50V) MLCCs using X5R and X7R dielectric materials (Fig. 3.(c)&(d)). The dielectric thickness is measured using SEM.

Fig. 3.(c) and (d) when investigating the low-voltage families (16V-50V). As can be seen, the relation between t and V_{rated} becomes irregular for low-voltage samples. Notably, the dielectric thickness of a 16V MLCC (C2012X5R1C225K125) is higher than that of a 50V sample (C2012X5R1H475K125) using the same dielectric material. Such outliers were previously mentioned in [16] and can be attributed to the emphasis on mechanical stiffness over energy density in low-voltage MLCCs, considering the mechanical fragility of the Class II dielectric material [16], [17]. To counteract the capacitance reduction when a bias voltage is applied is another reasonable motivation to retain a dedicated thickness of the dielectric.

Meanwhile, the dependence of Steinmetz's parameters on DC voltage bias deserves much attention, as Class II MLCCs are widely used in high-voltage-bias applications like DC-link capacitors and resonant capacitors illustrated in Fig. 1. However, there are no definitive conclusions on this topic yet. According to the experimental results of a limited number of MLCC samples, the dependence of power loss on DC bias has been ignored [2]. Opposite results have also been observed that, at a certain current level, power loss increases remarkably when a high bias voltage is applied [9]. This phenomenon, however, remains unexplained by the bias-independent ferroelectric hysteresis loss model, necessitating more accurate characterization methods and modeling tool to facilitate the loss prediction in resonant converters where the MLCCs are highly polarized.

C. Summary

As aforementioned, the existing characterization circuits and modeling approaches for Class II MLCCs have significant limits, preventing them from accurately capturing the actual loss profile of MLCCs, in particular, under high-frequency excitation and DC-biased applications. Furthermore, the lack of material-specific information hinders the development of a generalized loss model analogous to that of magnetic material, i.e. loss per unit volume can be derived directly from material loss parameters and applied excitations [18].

III. Experimental Setup and Large-signal Loss Characterization

A. Proposed Res-ST Circuit for Large-signal Characterization

To overcome the summarized issues, this paper presents a novel Res-ST circuit tailored to apply desired excitations on CUTs, representing realistic operating conditions in typical high-frequency resonant converters. As illustrated in Fig. 4. (a) and (b), the test setup is developed from a 1:1 resonant switched-capacitor circuit, in which the resonant tank is reconstructed and a DC bias voltage is introduced. The upper (red) and lower (blue) switches are driven ON/OFF with complementary PWM signals. In the resonant tank, the cascaded combination of the CUT and the reference capacitor C_{REF} is connected in series with the resonant inductor L_{RES} to form a resonant ST circuit, which operates at a resonant frequency f_{res} given by:

$$f_{res} = 1 \Big/ 2\pi\sqrt{L_{res}\frac{C_{REF}\cdot C_{CUT}}{C_{REF}+C_{CUT}}} \tag{2}$$

The testing frequency can be adjusted flexibly from hundreds of Hz to several hundred kHz by varying the value of L_{RES}. The proposed Res-ST circuit behaves as a current source due to the charge balance in the periodic steady state of a switched-capacitor circuit [19]. Hence, the excitation current is bound by the load current $i_o = V_o/R$ as $i_{RMS} = (\pi \cdot i_o)/\sqrt{2}$ at the resonant frequency, resulting in an extensive range of excitation amplitude. This feature makes it particularly suitable for the characterization of high-capacitance capacitors at high frequency. Moreover, DC bias voltages V_{bias} can be applied to the CUT from an external power supply.

In contrast to the V-I method which is used as a common procedure for $B-H$ loop characterization [20], this method represents essentially a V-V measurement since the charge on the CUT is reflected from the voltage across C_{REF}, as shown in Fig. 5. This setup eliminates the need for current measurements which are prone to errors compared to voltage measurements, through extracting the charge of the CUT from the voltage across C_{REF}. In the circuit, a bank of ten Class I

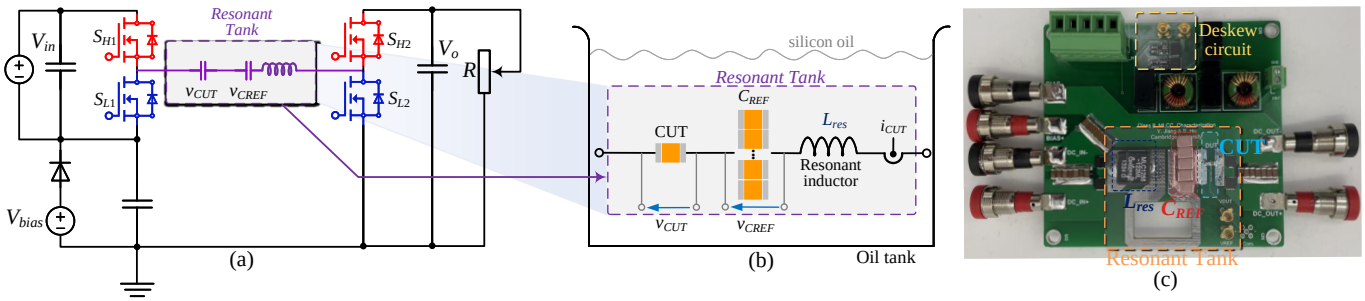


Fig. 4. Schematic of the Res-ST circuit and test setup. (a) Customized Res-ST circuit to adjust the excitation level applied on the CUT and its corresponding schematic composed of two half bridges, load and a resonant tank. (b) C_{DUT}, along with the entire resonant tank, is immersed in silicon oil tank which emulates different operating temperatures. The voltage across C_{CUT} and C_{REF} are both measured by Kelvin sensing. (c) Experimental circuit board with integrated deskew circuit are used to calibrate voltage probes.

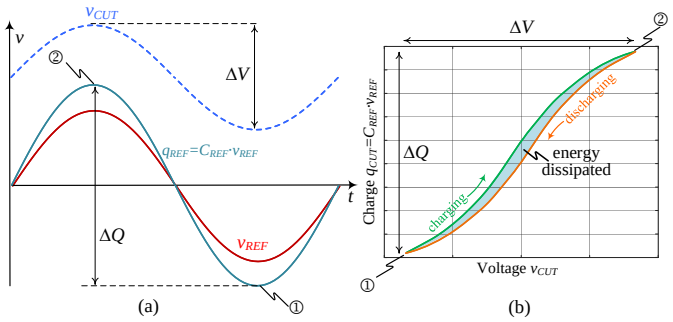


Fig. 5. Q-V loop obtained by the Res-ST circuit. (a) Obtained voltage waveforms across C_{CUT} and C_{REF} during one fundamental cycle. (b) Illustration of the nonlinear charge(Q)-voltage(V) curve by plotting v_{CUT} against v_{REF}, both obtained from (a). Circled numbers (① and ②) denote different points of time in the measurement.

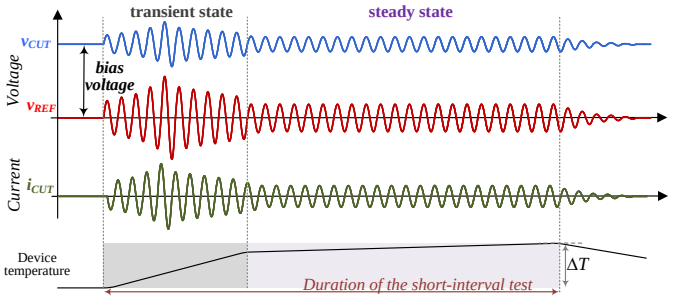


Fig. 6. Illustration of theoretical current and voltage waveforms in a short interval in which the temperature rise of the CUT is subdued.

MLCCs (CGA8R2C0G1H224J320KA) with a capacitance of 220 nF and a low dissipation factor (smaller than 2×10^{-4}) is employed as C_{REF} due to their linear relationship between voltage (v) and charge (Q). A 1MΩ resistor is parallelled with the reference capacitor bank to tune the ratio of DC equivalent parallel resistance (EPR) [2], ensuring a larger portion of the DC bias voltage would be allocated to the CUT. The voltages v_{CREF} and v_{CUT} across C_{REF} and CUT are measured individually by two differential probes.

Theoretical and experimental waveforms of the Res-ST measurement circuit are given in Fig. 6 and Fig. 7, respectively, demonstrating good agreement. In Fig. 7, the part number of the CUT is C5750X7R2E105K230, of which the capacitance is $1\mu F$. In experimental results, it can be seen that the CUT is biased by a 90V DC voltage and the peak value of the excitation current reaches 35A, corresponding to a peak excitation voltage of 73V. The resonant frequency at this operation point is 156kHz. Meanwhile, the output voltage remains at a relatively low value (<2V), which introduces low common-mode voltage as the grounding points of voltage probes are floating. The $Q-V$ curve of the CUT is obtained by plotting v_{CUT} against $q_{CUT}=v_{CREF}\cdot C_{REF}$, as shown in Fig. 5. (a), and the enclosed area of the $Q-V$ loop (c.f. Fig. 5.(b)) represents the power loss energy that the Class II capacitor dissipates during one fundamental cycle.

B. Temperature Control via Short-interval Test

Maintaining a constant ambient and capacitor temperature during measurement is essential, considering that $BaTiO_3$ ferroelectric material is highly temperature-sensitive [2]. As illustrated in Fig. 4. (b), in order to maintain the ambient temperature around the capacitor at 25°C, the entire resonant tank is placed in a temperature-controlled oil tank, immersed with Kryo 51 silicon oil, which has a high specific heat capacity of 1.63 kJ/(kg·K). In this manner, the ambient temperature of the CUT is considered invariable during the measurement.

The self-heating of the CUT is avoided by implementing a short-interval measurement lasting for a few fundamental cycles at the resonant frequency, as shown in Fig. 6 and Fig. 7. A trade-off is made here, considering that a longer measurement time is beneficial in improving the signal-to-noise ratio (SNR) of the measurement. The 4th-order Foster thermal network, shown in Fig. 8.(a), of MLCCs with various packages, i.e. SMD 2012, 3216, 3225, 5750, 2220, are firstly extracted from COMSOL finite-element (FE) simulation, to predict the transient temperature response at specific power losses. Then a safe measurement area (SMA) is defined as the boundary within which the short-interval duration should be strictly restricted under certain loss conditions. Thereby, the temperature rise would not jeopardize the accuracy of the measurement. The SMA curves, depicted in Fig. 8. (b), represent the maximum allowed measurement duration with a 0.5°C temperature rise restriction, corresponding to a 0.29% change in power loss [2]. In the FE simulation, the MLCC body is considered as a homogeneous block of the dielectric material. The heat capacity and thermal conductivity of $BaTiO_3$ are set to 434 J/(kg·K) and 2.61 W/(m·K), respectively. This

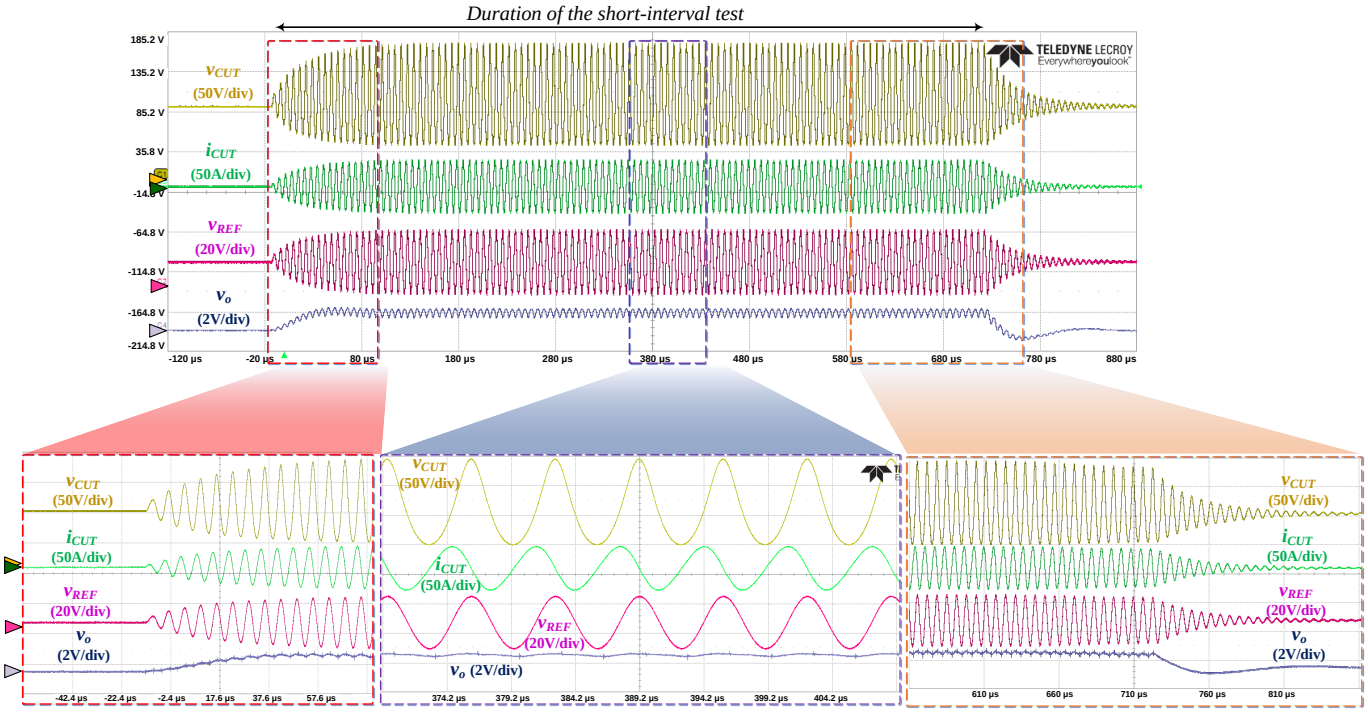


Fig. 7. Example excitation waveforms generated by the proposed Res-ST circuit in a short interval test. Key waveforms include the current waveform of the CUT: i_{CUT}, voltage waveform of the CUT: v_{CUT}, and voltage waveform of the C_{REF}: v_{CREF}. The part number of the CUT is C5750X7R2E105K230.

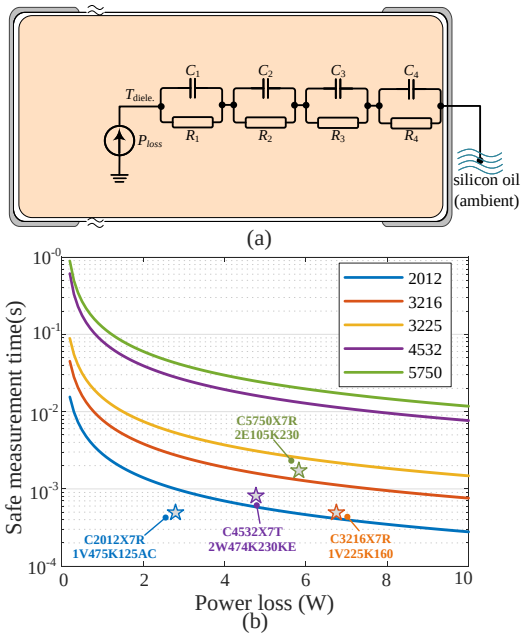


Fig. 8. (a) Thermal network of the MLCC, where the parameters of the structure-function [21] are extracted by finite-element analysis, and (b) Safe measurement area (SMA) for different MLCC packages of interest to determine the duration of the short-interval test.

setting represents a conservative estimation as the MLCC body contains a substantial amount of mass from the electrode plates made of nickel alloy, which has a much higher thermal conductivity (97.5 W/(m·K)).

IV. Large Signal Loss Characterization over Wide Frequency Range and DC Bias Voltage

The above-presented Res-ST test rig and procedure enable the large-signal loss measurement of Class II MLCC samples with flexible excitation. The measurements are performed by recording the voltages across the CUT and the C_{REF}, which are then mapped to the voltage (V) and charge (Q) of the CUT, respectively. In this section, the power losses of four CUTs with four different dielectric materials and rated voltages are first characterized under large-amplitude excitations and a wide range of frequencies. Then, the results from the loss measurement are used to extract the SE coefficient via curve fitting and to observe the influence of frequency and DC-bias voltage on loss behavior.

A. Large-signal Loss Characteristics under Varying Frequency and DC-bias Voltage

A series of hysteresis Q-V loops of four CUTs employing four dielectric materials marked as X5R-LV, X7R-LV, X7T-HV, and X7R-HV, respectively, are obtained by changing the positive DC biases supplied to the Res-ST circuit, as shown in Fig. 9. In this figure, sub-loops in the same plot are extracted from tests with fixed peak-peak voltage on CUT and similar test frequencies (74.43-83.20 kHz for X5R-LV; 95.21-116.6 kHz for X7R-LV; 43.86-62.6 kHz for X7T-HV; 120.4-183.5 kHz for X7R-HV), but different bias voltages. Thus, a combination of sub-loops provides a holistic hysteresis Q-V loop for each CUT. It is evident that these four samples exhibit various Q-V loop patterns, resulting in differences in large-signal loss characteristics, and the saturation of Q/V with increased DC-bias voltage leads to a decreasing capacitance.

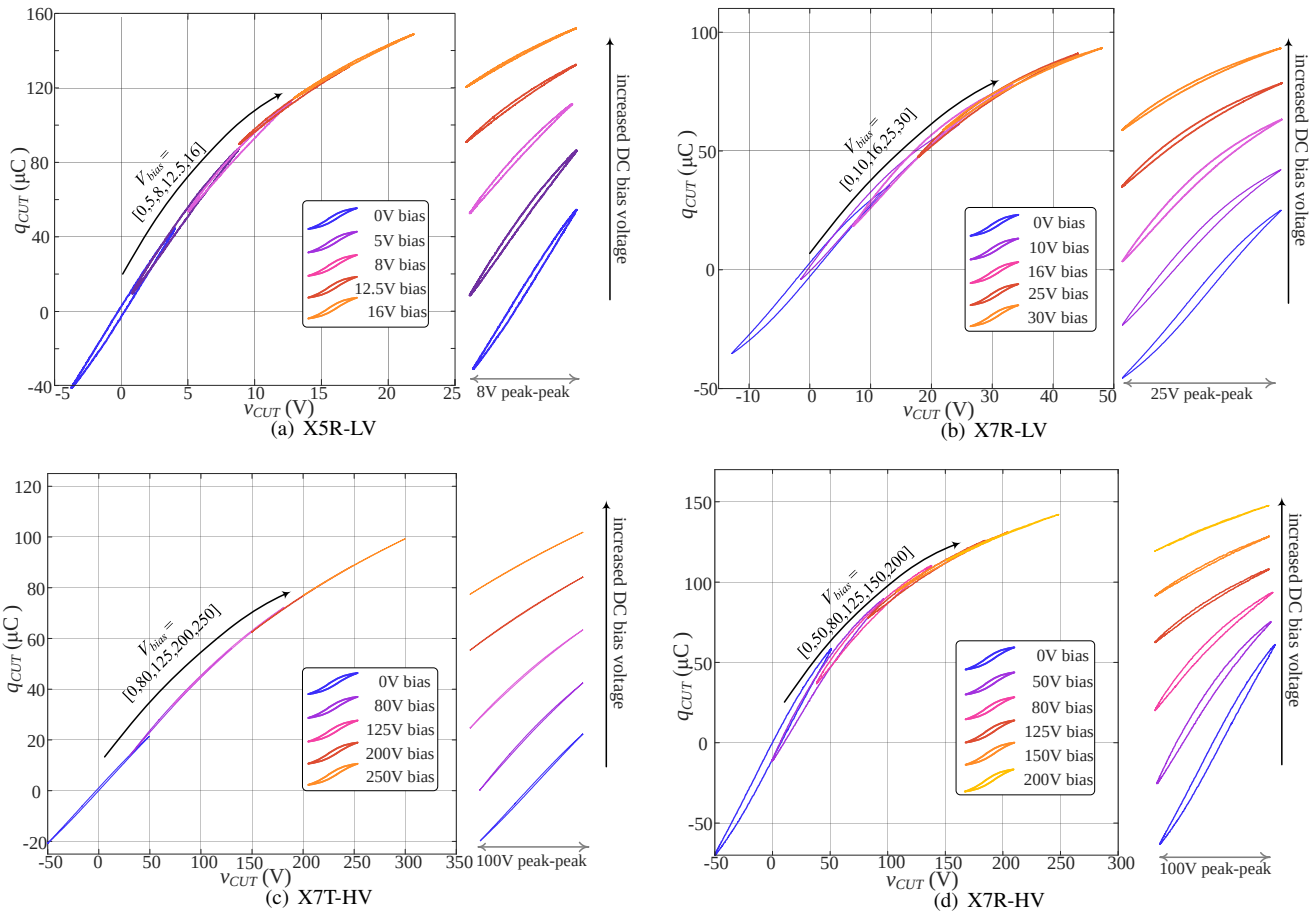


Fig. 9. Measured hysteresis loops with constant voltage peak value and increasing bias voltage. Q-V loops of (a) Low-voltage X5R sample (C3216X5R1E106K160) under an increasing bias voltage(0V, 5V, 8V, 12.5V, and 16V). (b) Low-voltage X7R sample (C3216X7R1V225K160AE) under an increasing bias voltage(0V, 10V, 16V, 25V, and 30V). (c) High-voltage X7T sample (C4532X7T2W474K230KE) under an increasing bias voltage (0V, 50V, 80V, 125V, 150V, and 200V.) (d) High-voltage X7R sample (C5750X7R2E105K230KE) under an increasing bias voltage (0V, 50V, 80V, 125V, 150V, and 200V.)

Therefore, it becomes possible to measure the MLCC loss behavior under varying DC voltage biases, excitation amplitudes, and frequencies. The large-signal losses of CUTs under each operating condition are calculated using the enclosed $Q-V$ areas per cycle and indicated as dots, as illustrated in Fig. 10. The losses of the MLCCs under the maximum and minimum frequency are fitted by the SE function and colored in blue and red, respectively, to demonstrate the trend of power loss behavior over frequency variation.

In Fig. 10, loss power/frequency, which physically represents the energy enclosed in an individual $Q-V$ loop, of the four samples over a wide range of frequencies is plotted against charge Q, and it can be seen that different types of dielectric materials exhibit distinct dependence on frequency and bias voltage. Specifically, the loss trend lines of the low-voltage X5R, X7R and high-voltage X7R move upward with increased DC-bias voltage, indicating a strong positive loss sensitivity to DC-bias voltage. Meanwhile, a positive correlation with frequency can be seen as well but the degree of dependency varies. The X7T-HV material, however, stands out as a special case as its dependencies on both DC-bias voltage and frequency variation are weak. At the same excitation level, i.e. Q_{pk}, the loss changes by less than 5% when the DC-bias voltage spans from 0 to 250V. This observation confirms the coexistence of both bias-sensitive and bias-insensitive dielectric material used in Class II MLCC. It also implies that the divergence between [2] and [9] regarding the DC-bias voltage dependence could be caused by the fact that dielectric materials with different recipes have been used but all are classified as Class II by manufacturers. It should be noted that the plotted loss were measured at a certain ambient temperature (25°C). Additionally, a significant decrease in loss at higher operating temperatures, in alignment with the findings in [2], was also observed.

It is also desired to analytically describe the losses considering the impact of the DC-bias voltage. However, Steinmetz's equation (SE) is only able to characterize hysteresis loops against different excitation amplitude. Therefore, based on the conventional SE, this paper proposes an improved method where a SE coefficient graph is built up to include the dependency of Steinmetz's parameters on the bias voltage. The concept is analogous to the Steinmetz Pre-magnetization Graph introduced in [22], which is widely used for evaluating the core loss of an inductor/transformer under DC bias.

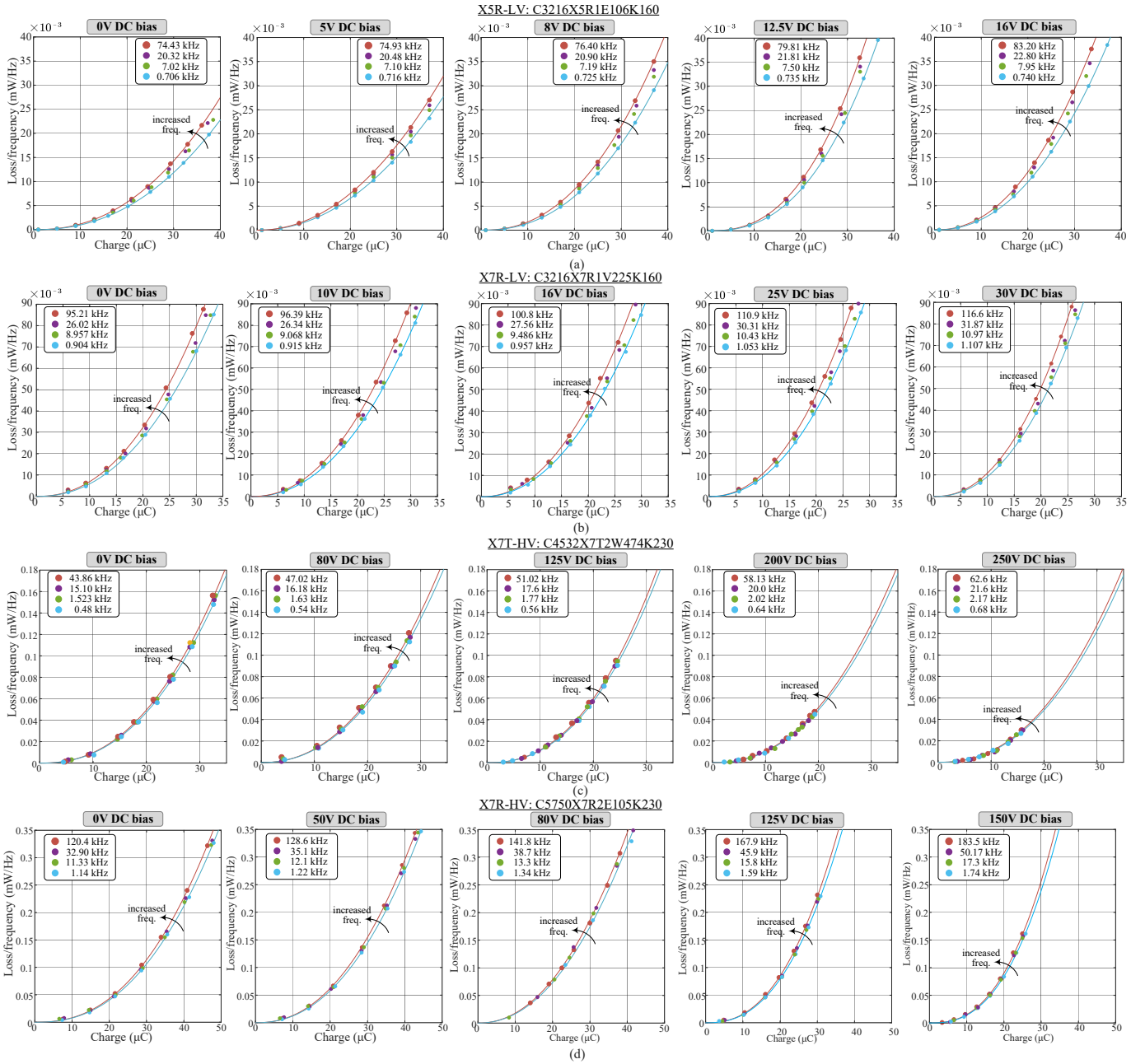
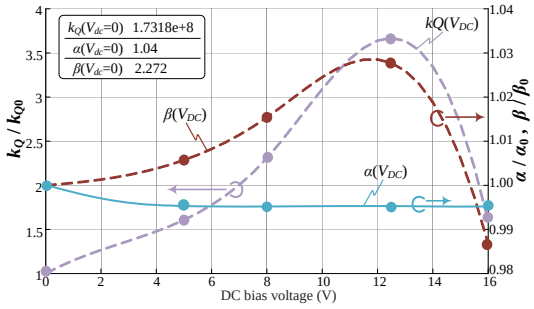


Fig. 10. Measured power loss/frequency (P/f), which physically represents energy enclosed per $Q-V$ loop, against measured charge Q_{pk} of 4 CUTs: (a) C3216X5R1E106K160 using LV X5R dielectric, (b) C3216X7R1V225K160AE using LV X7R dielectric, (c) C4532X7T2W474K230KE using HV X7T material, and (d) C5750X7R2E105K230KE using HV X7R material. In the test, both the frequency and the applied charge Q_{pk} were varied and different loss dependencies on frequency and DC-bias-voltage can be observed on these four types of dielectric materials.

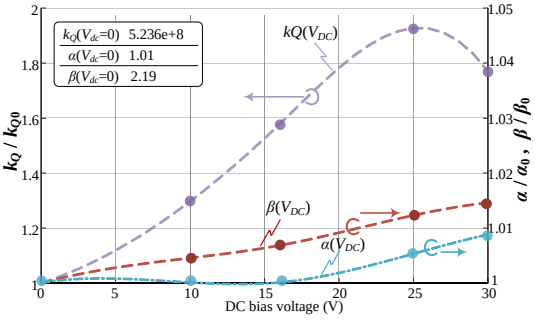
In the proposed graph, $\alpha(V_{DC})$, $\beta(V_{DC})$ and $k_Q(V_{DC})$ in the SE are considered as functions of DC bias voltage V_{DC}. α_0, β_0, and k_{Q0} are the SE coefficients to be experimentally extracted at zero bias voltage and used as reference values for normalizing $\alpha(V_{DC})$, $\beta(V_{DC})$, and $k_Q(V_{DC})$. The bias voltage is spanned from 0 to more than 60% of the rated voltage to be as inclusive as possible.

The SE coefficient graphs of four CUTs under different DC bias voltages are shown in Fig. 11. It is observed that the loss dependence on DC bias voltage varies among different dielectric materials. The frequency coefficient α in the SE is not obviously influenced by V_{DC}, valid on all four dielectric materials. The SE coefficients β and k_Q for X5R-LV, X7R-LV, and X7R-HV exhibit high sensitivity to the DC voltage, whereas X7T-HV material shows great independence from the DC bias voltage applied. The loss characteristic of the X7T-HV material changes only less than 5%, when the DC bias voltage is increased from 0V to 250V. The corresponding coefficients in SE, i.e. k_Q and β, have insignificant changes as a consequence. It should be noted that, for all CUTs, even minor changes in $\beta(V_{DC})$ can have a considerable influence on loss estimation.

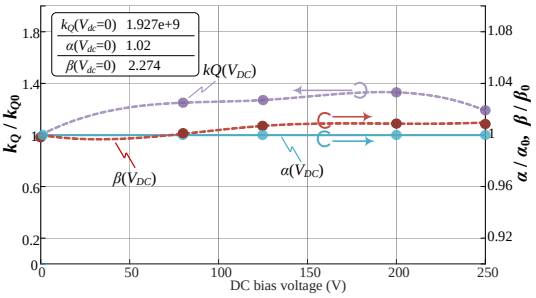
To visually demonstrate the effect of DC bias voltage on various dielectric materials, Fig. 12 interprets high-frequency



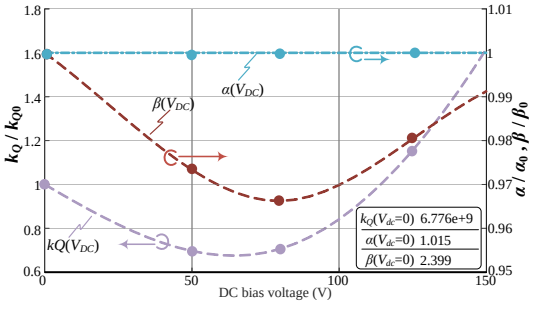
(a) C3216X5R1E106K160: X5R-LV



(b) C3216X7R1V225K160: X7R-LV



(c) C4532X7T2W474K230: X7T-HV



(d) C5750X7R2E105K230: X7R-HV

Fig. 11. Changes of the coefficients in Steinmetz's equation according to varying DC bias voltage.

measurement results from Fig. 10, where power loss/frequency (P/f) is plotted against charge (Q), in terms of ESR values at various current and DC bias voltages. It is important to note that the variation in measurement frequency at different DC bias voltages shown in Fig. 10 has been normalized by the frequency coefficient α. It is evident from the figure that the ESR of all four MLCC samples gradually increases with higher load currents. Furthermore, an increase in DC bias voltage results in a higher ESR at the same current level for X5R-LV, X7R-LV, and X7R-HV dielectric materials. However,

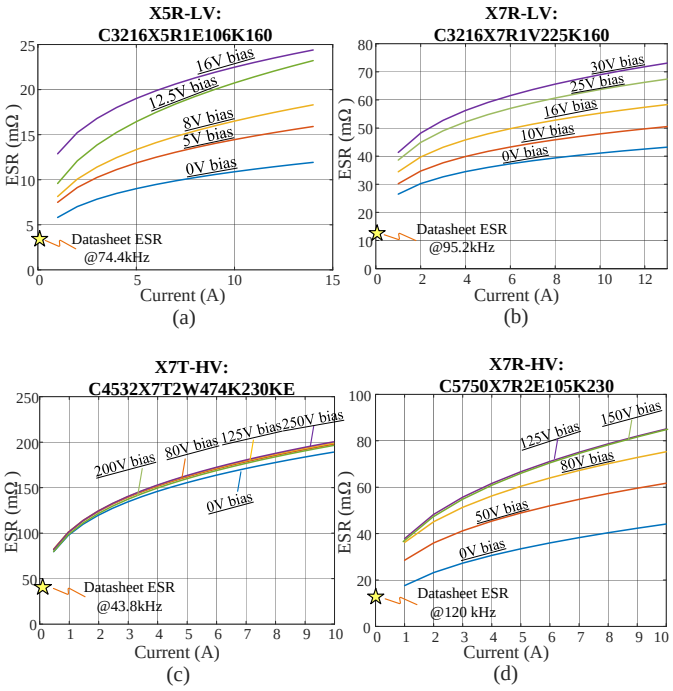


Fig. 12. ESR characteristics of four Class II MLCC samples at high frequency with various DC bias voltages: C3216X5R1E106K160(@74.4 kHz), C3216X7R1V225K160(@95.2 kHz), C4532X7T2W474K230KE(@43.8 kHz) & C5750X7R2E105K230(@120 kHz)

X7T-HV is unaffected by variations in the applied bias voltage, as its ESR remains stable. Additionally, the figure displays the small-signal ESRs provided in the datasheet for each subplot. It can be observed that the discrepancy between the large-signal and small-signal ESR values is minimal at low currents, but increases significantly at higher load conditions.

B. From Device-specific to Material-specific Loss

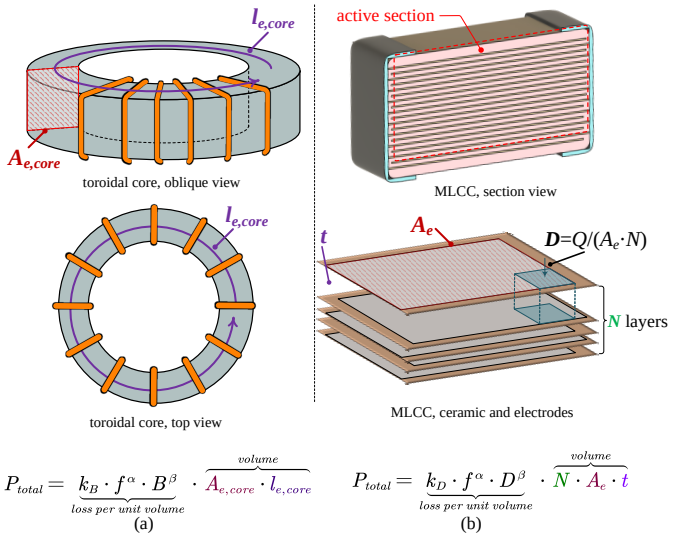


Fig. 13. Analogy between a typical toroidal core inductor and an MLCC, where B-based and D-based loss estimation methods are used, respectively.

The measurement results presented above primarily focus on device-specific parameters using the Q-V loop. Its generalization to other commercial devices, even having the same dielectric material, is limited. Nevertheless, it is worth noting that the loss mechanisms for magnetic core and MLCC dielectrics share similarities, as they both originate from the hysteresis loop, whether magnetically or electrically. Consequently, the loss modeling of MLCC can be expanded from the device level to a more fundamental material level by drawing insights from previous research conducted on magnetic components.

In the loss estimation of a magnetic component using homogeneous material, a B(flux-density)-based Steinmetz's loss equation is preferred by engineers, and material-specific loss information (loss per unit volume/weight) is usually provided for this equation by manufacturers. By incorporating knowledge of the device's geometric dimensions, the losses of the magnetic component of interest under specific excitation can be directly estimated. As depicted in Fig. 13. (a), such a manner is conveniently achieved on a toroidal core power inductor as both the path length ($l_{e,core}$) and cross-section area ($A_{e,core}$) are easy to access. As a result, with the available material-specific loss information, loss estimations can be made for all devices utilizing the same material.

With an attempt to apply this principle on an MLCC with a multilayered structure, an analogy is given in Fig. 13 to illustrate both commonalities and differences. Similar to the B-based SE, the loss of an equivalent capacitor can be alternatively represented in the form of a $D-$(displacement field)-based SE [8]

$$P = \rho \cdot V_{ol} = k_D \cdot f^{\alpha} \cdot D_{pk}^{\beta} \cdot V_{ol} \tag{3}$$

where ρ is the loss density, V_{ol} denotes the volume of the device and $D = Q/(N \cdot A_e)$ represents the electric displacement field. Therefore, this D-based SE is a dielectric material-specific model and has the potential to be generalized to evaluate all devices using the same dielectric material. To achieve complete generalization, accounting for the complex MLCC structure, three parameters are necessary: layer number (N) and overlapping area (A_e) of each layer to derive the D, and additionally dielectric thickness (t) for calculating the volume. These three parameters are correlated by: $C_{rated} = \varepsilon_0 \frac{A_e \cdot N}{t}$ where C_{rated} is the nominal capacitance and ε_0 is the dielectric constant.

As C_{rated} is readily accessible from the datasheet and ε_0 is a device-invariant material property, knowing the value of t allows us to determine $A_e \cdot N$. Consequently, the three geometric parameters (N, A_e, and t) can be gradually decoupled. The exact value of t, however, now stands out as the only unknown quantity, which is unfortunately rarely published by manufacturers. Using the rated voltage to speculate t is not physically supported by the survey in Fig. 3, particularly for low-voltage families. Meanwhile, although it is possible to conduct cross-section analysis on specific samples, repeating this equipment-intensive process for every single device is rather unrealistic given the vast number of MLCCs available on the market. Therefore, it is imperative to employ an efficient yet simple analysis to extract internal geometry information, i.e. N, t, and A_e. These parameters will facilitate the normalization of Q-based SE coefficients to their D-based counterparts, effectively extending the device-specific loss model to a material-specific format.

To demonstrate how the material-specific loss information will be built in the following section, a flow chart outlining the entire process of describing the loss characteristics of dielectric material is given in Fig. 14.

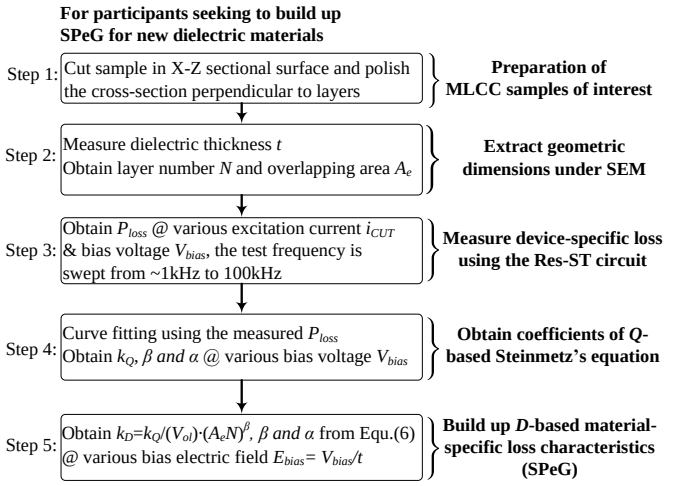


Fig. 14. Process for establishing the loss characteristic of new ferroelectric dielectric material.

V. Dielectric Thickness Observer (DTO) Bridging Small-signal and Large-signal Measurement

Accordingly, this paper presents a method to disclose dielectric thickness (t) by using SEM, and such destructive analysis is only required to be conducted once on one of the devices using the same dielectric material. Then, an easy-to-follow tool, dielectric thickness observer (DTO), is also introduced in this section to allow users to speculate t effectively without the need for further micro-structural observation.

A. Working Principle of SEM and Preparation of Samples

The SEM is a type of electron microscope which generates images by scanning the surface with a focused beam of accelerated electrons. The emitted electrons interact with atoms in the sample, and those back-scattered electrons are collected to produce images. Compared to an optical microscope, the SEM is featured by high resolution, greater depth of field and the ability to different materials with similar optic characteristics, such as ceramics used for shell and dielectric in a MLCC. These features make SEM ideal for characterizing both magnetic [23] and dielectric components with delicate and complex structures.

The working mechanism of SEM requires careful sample preparation before scanning. MLCCs are manufactured by the co-firing of ceramic and nickel layers. While the nickel electrodes have high conductivity, that of the dielectric material is usually poor. The no-conductive dielectric material collects charge when scanned by the electron beams, and this phenomenon, also known as charge accumulation, causes scanning

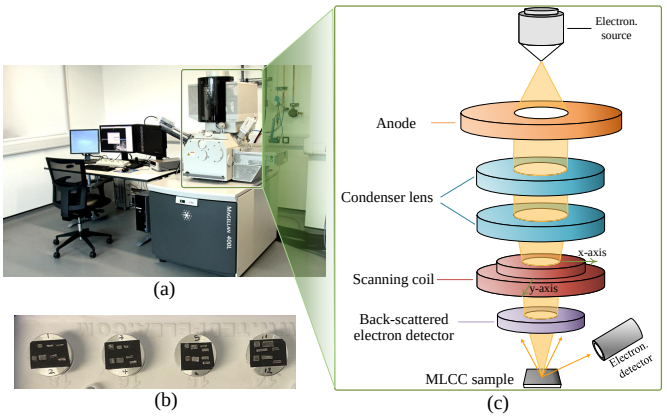


Fig. 15. (a) Magellan 400 SEM used to image the micro-structure of MLCC samples, (b) Prepared MLCC samples which are mounted on a grounded aluminum holder, and (c) Simplified schematic diagram of SEM.

faults and image artifacts. To prevent charge accumulation, the prepared MLCC samples should be mounted on electrically grounded metal plates through a thin layer of carbon adhesive tapes, as illustrated in Fig. 15.(b). The MLCC samples are cut in the X-Z sectional surface to access t, N and overlapping length. In Fig. 16, SEM images on both high-voltage and low-voltage samples are given. As can be seen, proper preparation ensures high image resolution, and geometric information of the samples is easily accessible. Additional SEM images of CUTs are provided in the supplemental document.

B. Proposed DTO Bridging Small-signal and Large-signal Measurements

The dielectric thickness t of an MLCC is essential in making use of the material-specific loss information to estimate the loss of a certain device. The SEM is advantageous in capturing MLCC's geometrical parameters with ultra-high accuracy. However, its limited availability hinder the popularization of such a loss model. In order to address this issue, we propose a new method, dielectric thickness observer (DTO), to estimate the dielectric thickness of MLCCs using their small-signal C-V characteristic, which is usually accessible from the product datasheet.

Due to its inherent nonlinear nature [24], the ferroelectric material's dielectric constant ε is highly sensitive to the DC electric field E applied. Notably, a strong negative correlation can be seen in $BaTiO_3$-based dielectric material, and such dependence has been referred to as a ε-E dependence. This standalone material property is independent of the MLCC package [25], e.g. layer number N and active area A_e of each layer. Meanwhile, the electric filed E will be determined by both internal dielectric thickness t and applied DC-bias voltage externally. When the dielectric material is packaged into a MLCC, the ε-E dependence is manifested in the form of capacitance-dc-bias-voltage (C-V) dependence which is readily available from the DC Bias characteristic in the manufacturer's datasheet.

The ε-E and C-V characteristics are correlated by: $C = \varepsilon \cdot \frac{A_e N}{t}$ and $V = E \cdot t$, respectively. Therefore, if the ε-E dependence of a certain dielectric material, e.g. X5R, X7R or X7T, is known, it can serve as a reference to speculate the dielectric thickness of counterparts using the same material without conducting destructive cross-section analysis, given that the C-V characteristics have been known.

Fig. 17 illustrates the flowchart of the proposed DTO. Initially, the C-V characteristic of the CUT is acquired either from the datasheet or through small-signal measurements using a Vector Network Analyzer (VNA). Subsequently, the $C(V_{DC})$-V_{DC} curve is normalized to the $C(V_{DC})/C_0$-V_{DC} characteristic of the CUT by substituting $C(V_{DC})$ with $C(V_{DC})/C_0$, which ranges from 0 to 1. Here, C_0 represents the capacitance of the CUT at zero bias voltage and $C(V_{DC})/C_0$ denotes the normalized effective capacitance at bias voltage V_{DC}. Since capacitance C is given by $\varepsilon \cdot \frac{A_e N}{t}$, the normalization process cancels out the influence of A_e, N, and t as they are independent of E field applied, thus retaining the effect of relative permittivity ε only. In the next step, an initial value of the estimated dielectric thickness $\widehat{t}$ is used to convert the bias voltage V_{DC} into the corresponding bias electric field $\widehat{E_{DC}}$ via $\widehat{E_{DC}} = V_{DC} \Big/ \widehat{t}$. Subsequently, the $C(V_{DC})/C_0 - V$ characteristic is transformed into $C(\widehat{E_{DC}})/C_0 - \widehat{E_{DC}}$, and then into $\varepsilon(\widehat{E_{DC}})/\varepsilon_0 - \widehat{E_{DC}}$ characteristic, representing the normalized effective dielectric constant under various electric fileds. Importantly, since the capacitance $C(V_{DC})$ has been normalized to $C(\widehat{E_{DC}})/C_0$, the $\varepsilon/\varepsilon_0$ can be directly obtained in this step as it holds the same value as C/C_0, under the same electric field.

With a proper estimation of dielectric thickness $\widehat{t}$, the estimated $\varepsilon(\widehat{E_{DC}})/\varepsilon_0$-$\widehat{E_{DC}}$ characteristic should exhibit the same shape as the true one of the dielectric material, and the relative distance between the estimated $\varepsilon/\varepsilon_0$-$\widehat{E}$ curve and the pre-known true one, which is package-independent, is expected to be zero. Therefore, an error function is defined to describe the distance between these two competing curves:

$$error = \sum_{k=1}^{N_{C-V}} \left[f_{\varepsilon,E}\left(\widehat{E_k}\right) - \frac{\varepsilon_k}{\varepsilon_0} \right]^2 \tag{4}$$

where $f_{\varepsilon,E}$ is a pre-known analytical function describing the $\varepsilon/\varepsilon_0$-$E$ dependence of the material, $\widehat{E_k}$ and $\frac{\varepsilon_k}{\varepsilon_0}$ is a pair of estimated electric field strength and normalized effective permittivity at this certain electric field strength, both obtained from the previous step, and N_{C-V} is the number of data points in the C-V curve provided in the datasheet. The estimation error is then fed to an optimizer and converges to the $\widehat{t}$ with the least error after iterations.

In order to implement the proposed DTO, the ε-E characteristic of multiple dielectric materials from TDK has been extracted and presented in Fig. 18. These ε-E characteristics are captured by normalizing a cluster of $C-V$ coordinates from datasheet, after knowing all the necessary geometrical information of the internal structure, i.e. t, N and A_e. To analytically describe the dependence of ε on electric field strength E, a modified Johnson's formula, which is firstly unveiled in [26], is used to achieve such a purpose:

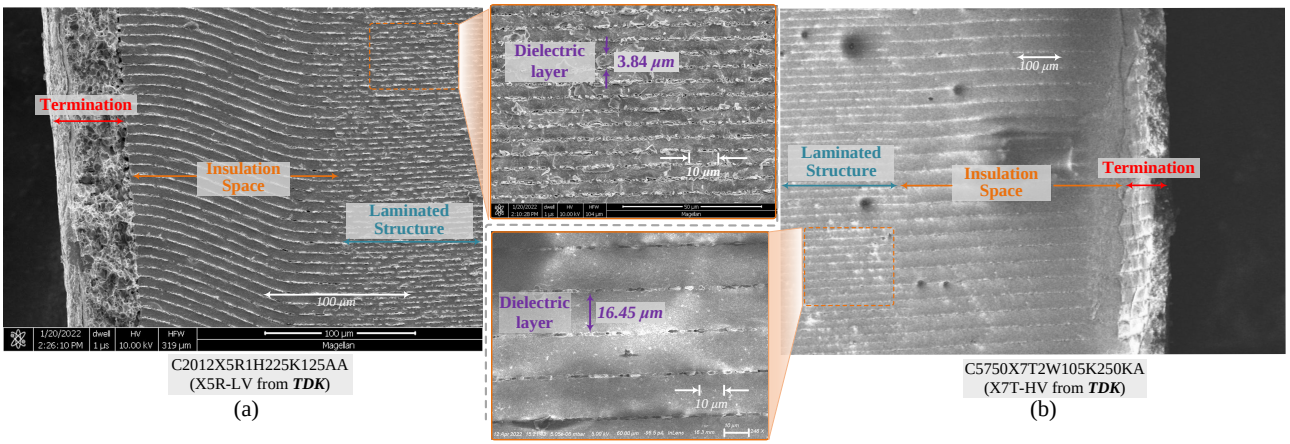


Fig. 16. Cross-sectional SEM images of two typical MLCC samples: (a) a low voltage X5R sample (C2012X5R1H225K125AA), and (b) a high voltage X7T sample (C5750X7T2W105K250KA) from TDK.

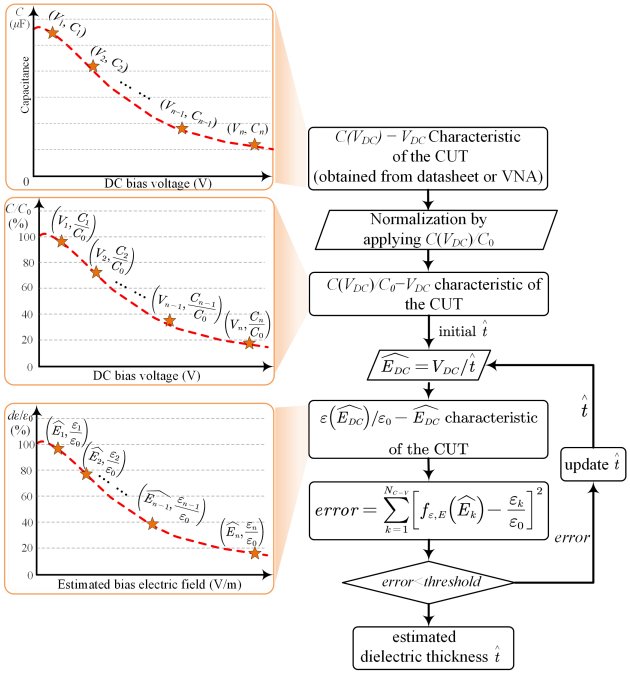


Fig. 17. Working flow of the proposed DTO: $C-V$ characteristic is fed as input to the DTO and estimated dielectric thickness is yielded as the output.

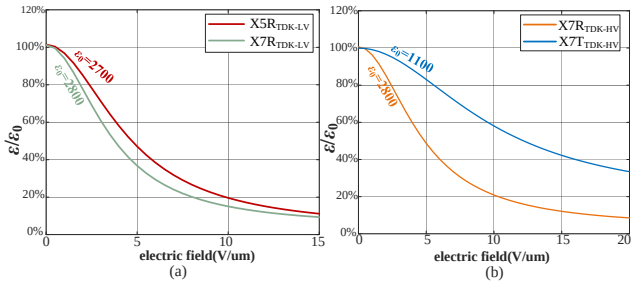


Fig. 18. Comparison of the ε-E characteristics of 4 types of dielectric materials from TDK. (a) LV X5R and LV X7R used in low-voltage MLCCs. (b) HV X7R and HV X7T used in high-voltage MLCCs.

TABLE II
PARAMETERS OF DIELECTRIC MATERIALS INVESTIGATED FITTED BY THE JOHNSON'S FORMULA [26]

Material \ Parameters	γ	δ	ε_{00}	ε_0
X5R-LV	1.015	5.019×10^{-2}	0.0303	2700
X7R-LV	1.029	7.439×10^{-2}	0.0417	2800
X7T-HV	1.209	1.243×10^{-2}	0.1726	1100
X7R-HV	1.032	4.920×10^{-2}	0.0618	2800

$$\varepsilon(E) = \varepsilon_0 \left(\varepsilon_{00} + \frac{1}{\gamma + \delta E^2} \right) \tag{5}$$

where ε_{00}, γ and δ are characteristic constants of each material. ε_0 is the dielectric constant at zero bias electric field strength.

The DTO relies on small-signal C-V characteristics of the MLCC as input data. These characteristics can be obtained either from the manufacturer's datasheet or by performing a one-port (S_{11}) measurement, as illustrated in Figure 19. The datasheet provides a set of discrete [C, V] coordinates describing the voltage-dependence of the sample. However, if the density of coordinates is limited or the information is not provided at all, a VNA and a DC bias injector (e.g., Picotest-J2130A) can be used to perform a one-port S-parameter (S_{11}) measurement with a bias voltage. The calibration and measurement procedures for the S_{11} measurement are detailed in [27] and [28]. The performance of the DTO fed by [C, V] coordinates obtained from a VNA is evaluated in the supplementary material of this work, and the comparison between DTOs using VNA and datasheet [C,V] information is presented in Table A1, demonstrating similar results and good estimation accuracy. It should be emphasized that the S_{11} measurement is based on the output voltage ratio of Port 1 to the voltage input of Port 1. Therefore, the injected DC bias should not alter the essence of a one-port measurement.

C. Performance of the Proposed DTO

To be more generic, capacitors were selected to encompass a vast range of package sizes, rated DC voltage, and capacitance.

31 samples from 4 types of dielectric materials were used as test datasets in this paper. The cross section of these samples was firstly imaged under SEM to extract their t. Then, their C-V curves were fed to the proposed DTO to generate their corresponding $\widehat{t}$. A comparison between the estimated $\widehat{t}$ and the measured t is given in Appendix Table. A1, A2, A3, and A4. According to the comparison, the DTO is able to achieve a high estimation accuracy with mean errors of 2.1%, 1.975%, 2.65% and 3.31% for X5R-LV, X7R-LV, X7R-HV and X7T-HV materials, respectively. The MATLAB scripts of the DTO have been included as part of the supplemental material for the manuscript.

D. SpeG Describing Material-specific Loss Information

Knowing both the device-specific loss and corresponding geometric information unblocks normalizing the loss information at material level, i.e. the power loss per volume of a certain ferroelectric material under arbitrary excitation. The conversion from device-specific SE coefficients to material-specific ones has been given in [2] and the process is simplified here as:

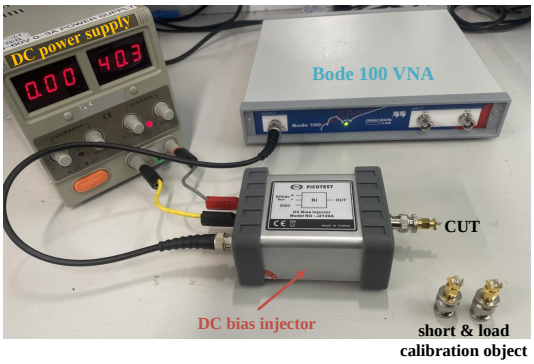


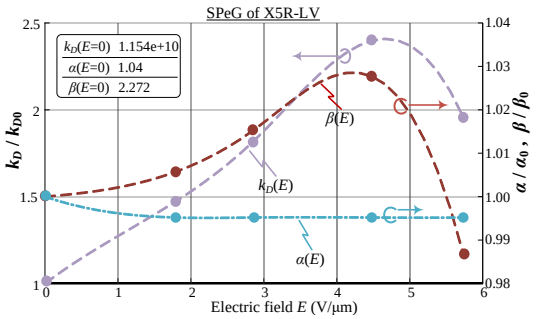
Fig. 19. Small-signal capacitance measurement with the presence of DC bias voltage using one-port (S_{11}) measurement. Short, load and open calibration objects are needed to ensure accuracy.

$$P = \overbrace{k_Q \cdot f^{\alpha} \cdot Q_{pk}^{\beta}}^{loss\ per\ device} = \underbrace{k_D \cdot f^{\alpha} \cdot D_{pk}^{\beta}}_{loss\ per\ voume} \cdot \underbrace{V_{ol}}_{volume} \tag{6}$$

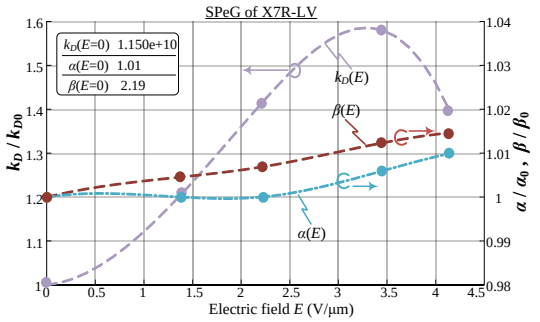
$$\xrightarrow{Q=A_e \cdot N \cdot D} k_D = \frac{k_Q}{V_{ol}} \left(\frac{Q_{pk}}{D_{pk}}\right)^{\beta} = \frac{k_Q}{V_{ol}} \left(A_e \cdot N\right)^{\beta}$$

where k_Q and k_D are the first coefficients in the device-specific and material-specific SEs, respectively. Note that the coefficients α and β remain the same in both device- and material-specific SEs. Subsequently, the distributions of device-specific coefficients in the SE equation given in Fig. 11 have been converted to their material-specific counterparts, as shown in Fig. 20. Since the dielectric thickness has been known, Fig. 20 is able to reflect the variation of SE coefficients at different electric (E) fields, and this method is therefore referred as Steinmetz's Pre-electrified Graph (SPeG).

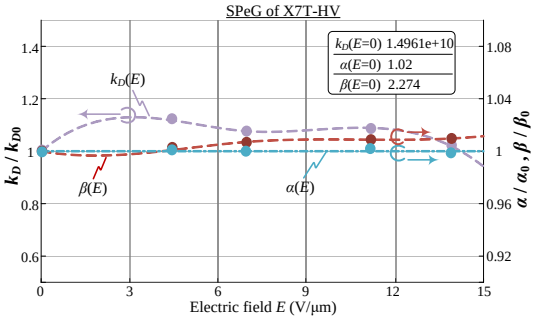
The SpeG quantifies the frequency and electric (E) field dependence of a specific material used for MLCC. Whenever the geometrical information of a certain MLCC is known, either from a destructive cross-section analysis or a non-destructive DTO, the SpeG enables the generation of power loss information for the MLCC device.



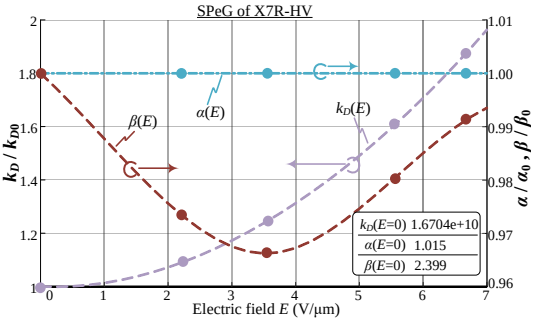
(a) X5R-LV



(b) X7R-LV



(c) X7T-HV



(d) X7R-HV

Fig. 20. SPeGs, which describe the effect of DC electric field bias on dielectric loss behavior, of four different materials: X5R-LV, X7R-LV, X7T-HV and X7R-HV, all from TDK.

VI. Device-level Validation and Loss Estimation for a Typical Resonant Converter

In this section, the proposed loss model is validated at both the device and converter levels. The device-level validation

examines the accuracy of the proposed SPeG when used in conjunction with the DTO, whereas the converter-level validation predicts the power loss of MLCCs in a practical resonant converter.

A. Device-level Validation

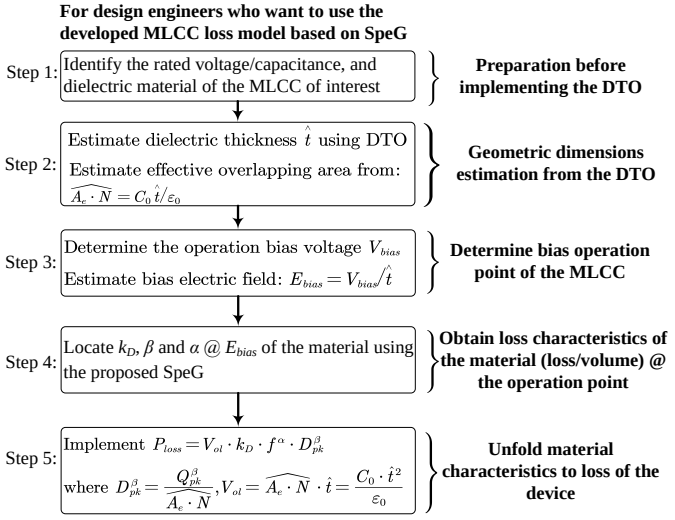


Fig. 21. Process for design engineers to calculate the MLCC loss by using material-specific parameters (SPeG).

To summarize the loss estimation process using the proposed model, Fig.21 provides an easy-to-follow guideline for users interested in directly implementing the proposed SPeG and DTO described in this paper. Following this flow chart, one is expected to identify the dielectric material used in the device of interest and then extract its geometric information using the proposed DTO. The corresponding material-specific loss characteristics depicted in SpeG, combined with the geometric information, will finally provides the loss per unit volume and then the loss of the entire MLCC.

For the device-level validation, one device from each material category (X5R-LV, X7R-LV, X7T-HV, and X7R-HV) was selected. For fair validation, these validation samples were deliberately selected to be of both different packages and capacitances from those used to develop the SPeGs. Their dielectric thickness t was firstly obtained from the DTO. Then, the SPeG was used to unfold the material-specific loss information, following the flow given in Fig. 21. The obtained material-specific SE coefficients from SPeG then enable the loss estimation at various operation frequencies and DC bias voltages.

We take C3216X5R1H106K160AB, whose loss prediction results will be given in Fig. 22. (a), as an example to provide a step-by-step process of loss prediction:

Step1 Preparation: The first step involves identifying the dielectric material and rated capacitance of the sample. In this case, the material is X5R-LV. The ε-E and loss characteristics of the material can be found in Fig. 18 and Fig. 20.(a), respectively. The rated capacitance is 10μF for C3216X5R1H106K160AB.

Step2 Geometric dimension estimation: Next, the dielectric thickness t and total overlapping area $A_e \cdot N$ of C3216X5R1H106K160AB are estimated using the proposed DTO, as detailed in Fig. 17, along with the accompanying MATLAB script in the supplemental material. The estimated dielectric thickness $\widehat{t}$ and overlapping area $\widehat{A_e \cdot N}$ of the sample are 3.16 μm and $1.3\times10^{-3}\mathrm{mm}^2$, respectively, as given in Table A1.

Step3 Determine operation point: The SPeG requires knowledge of the bias electric field. Thus, the corresponding bias electric field E_{bias} is deduced from $E_{bias} = V_{bias}/\hat{t}$, where $\widehat{t}$ has been estimated as 3.16 μm. In Fig. 22.(a), the loss behavior under three bias voltages (0V, 10V, and 15V) is investigated, and the corresponding E_{bias} values are $0\mathrm{V}/\mu m$, $3.15\mathrm{V}/\mu m$, and $4.74\mathrm{V}/\mu m$, respectively.

Step4 Locate Steinmetz's coefficients in SPeG: Once the operation point, i.e. E_{bias}, of the sample is known, the Steinmetz's coefficients, which represent the material-specific loss information and are functions of E_{bias}, can be located in the graphs illustrated in Fig. 20.(a).

Step 5 Generate device's loss: Finally, substituting the Steinmetz's coefficients (i.e. α, β, and k_D) of the X5R-LV material, provided in Step 4, and the geometric dimensions extracted in Step 2 into (6) yields the loss of C3216X5R1H106K160AB under various bias voltages and excitation levels.

The same Res-ST circuit was employed to measure the losses of the validation samples. A comparison between the estimated and measured losses was conducted both w/ and w/o DC bias voltage. In Fig. 22, the measured losses are scattered against the peak value of the charge, and the calculated power losses are plotted as a cluster of dotted lines. As can be seen, the estimated losses match with the measured losses with high accuracy across various excitations and DC bias voltages, with only a few exceptions at low excitation levels, which can be attributed to measurement error.

Unlike the estimation of core losses which is largely affected by the size and geometry of the core due to uneven magnetic flux distribution, that of a Class II MLCC shows low sensitivity to the device package. This feature can be attributed to the fact that it is easier to ensure an even distribution of D-field in an MLCC than B-field in a magnetic core, as long as dielectric thickness t remains uniform within one device and is significantly smaller than the electrode dimensions at the transverse plane, which is always the case for MLCCs.

B. Example of Loss Estimation for RSC Converters

A 2:1 resonant switched capacitor converter was built to apply the proposed loss model for Class II MLCCs on a real converter. The prototype serves as the basic building block within a larger architecture, e.g. the first/second stage in a cascaded 48V-24V-12V structure or the fundamental units in an N:1 converter, and is therefore selected due to its representativeness. Operation principles of a RSC has been extensively described in pieces of literature [29], [30]. The accuracy of the loss model can be examined by comparing the calculated and measured power losses.

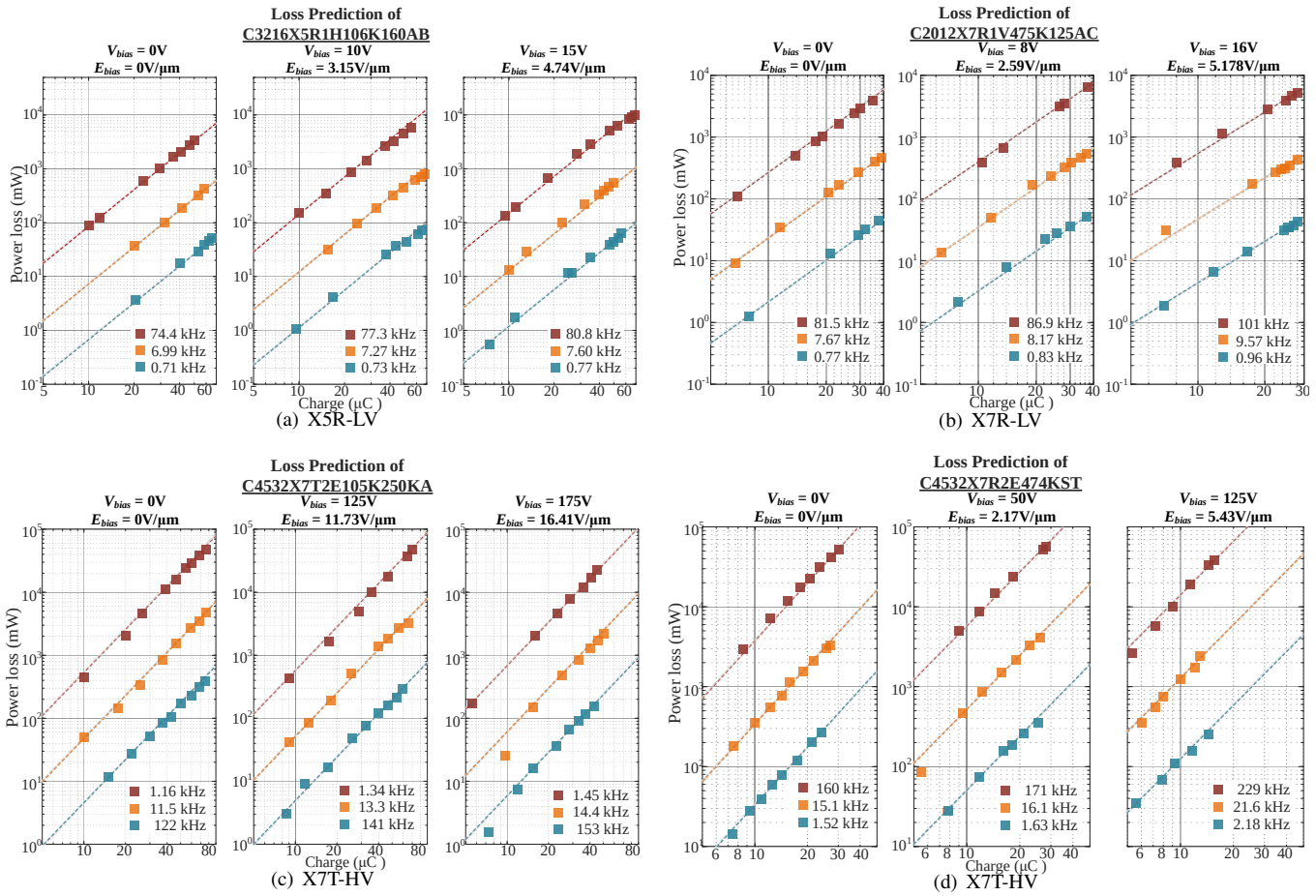


Fig. 22. Logarithmic representation of measured power loss against peak-peak charge Q_{pk} with an increased DC bias voltage. Squares represent the measurement results and dotted lines denotes the calculated power losses using the material-specific SE coefficients obtained from the SPeGs given in Fig. 20.

.

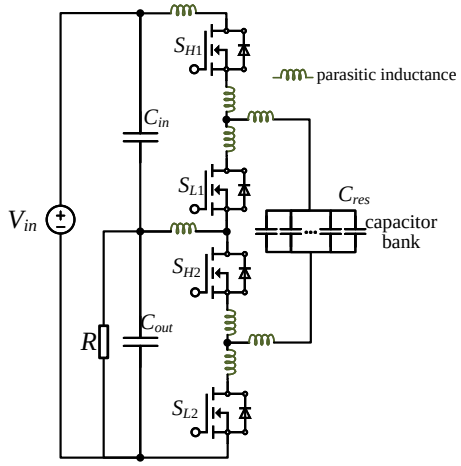


Fig. 23. Equivalent circuit of the magnetic-free 2:1 resonant switch-capacitor converter.

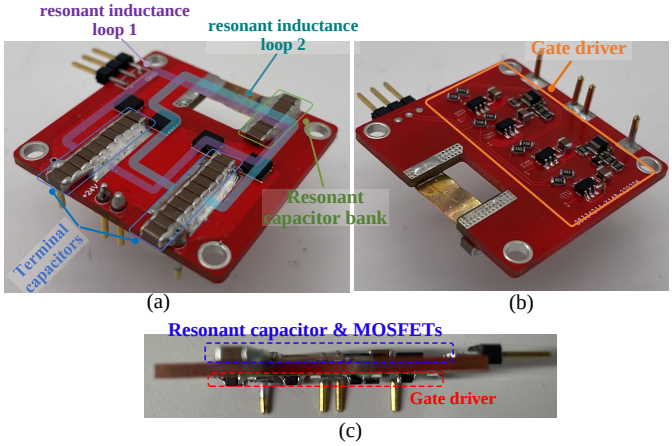


Fig. 24. Hardware prototype of the magnetic-free 2:1 switched resonant-capacitor converter. Annotated photograph of (a) the top layer where the parasitic inductance loops are denoted, and (b) the bottom layer of the printed circuit board. (c) The sectional view of the prototype.

As the resonant tank is in series with two MOSFETs at any moment, it is more intuitive to calculate the power loss using ESR instead of a Q-based loss model, with a conversion derived in [31]. Therefore, the charge-based loss model is converted to an ESR with the following derivation in the first step.

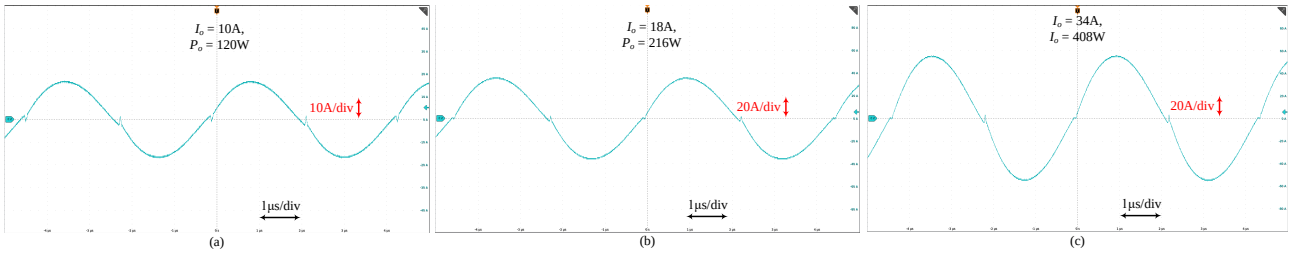


Fig. 25. Current waveforms through the resonant tank at various load conditions. (a) I_o=10A; (b) I_o=18A; (c) I_o=34A.

$$
\begin{aligned}
P_{loss} &= k_Q \cdot f^{\alpha} \cdot Q_{pk}^{\beta} = k_Q \cdot f^{\alpha} \cdot \left(\frac{\sqrt{2} i_{RMS}}{2\pi f} \right)^{\beta} \\
&= k_Q \cdot f^{\alpha-\beta} \cdot \left(\frac{1}{\sqrt{2}\pi} \right)^{\beta} \cdot (i_{RMS})^{\beta} \\
\Longrightarrow R_{\mathrm{ESR}} &= P_{loss} / (i_{RMS})^2 = \frac{k_Q}{(\sqrt{2}\pi)^{\beta}} \cdot f^{\alpha-\beta} \cdot (i_{RMS})^{\beta-2}
\end{aligned} \tag{7}
$$

According to the expression of R_{ESR}, the ESR of the MLCC is a function of current i_{RMS}, and it is expected to see an increased ESR with higher current, as β is always slightly higher than 2.

The resonant switched-capacitor converter experiences four types of power losses, namely semiconductor loss (which includes gate charge loss), inductor loss, stray loss (mainly composed of PCB trace loss), and capacitor loss. In this particular RSC prototype, the resonant frequency has been meticulously adjusted to ensure zero current switching (ZCS) throughout the entire load range, as illustrated in Figure 25. This means that the estimation of semiconductor switching loss can be reduced to calculating the junction capacitance (C_{oss})-related loss and gate driver loss. To avoid inaccurate loss estimation of discrete inductors with ferrite cores, parasitic inductances from device packages and PCB traces are utilized as the resonant inductor. This ensures that the only component exhibiting hysteresis behavior in the resonant tank is the MLCCs. The resonant tank has been designed with balanced loop inductance, as evidenced by the two highlighted loops in Figure 24(a), and the actual operating current waveforms presented in Figure 25. Consequently, the inductor loss and PCB ohmic trace loss are merged. The PCB trace resistance was determined through Ansys Q3D at the switching frequency.

Note that the terminal (input/output) capacitance of the prototype is only twice the resonant capacitance, which seemingly violates the practice that terminal capacitance should be considerably higher in an RSC converter. As a result, both C_{in} and C_{out} are involved in the resonant behavior [32], and their impact should be included by calculating their losses separately. Considering all these measures, the total power loss of the converter is expressed as:

$$
\begin{aligned}
P_{tot.} = {} & 2 \cdot i_{RMS}^2 \cdot R_{ds,ON} + R_{PCB} \cdot i_{RMS}^2 + 4 Q_{oss} V_o f_{sw} \\
& + \frac{R_{\mathrm{ESR}}(\frac{i_{RMS}}{N_{res}})}{N_{res}} \cdot i_{RMS}^2 + \frac{R_{\mathrm{ESR}}(\frac{i_{RMS}}{N_{term.}})}{N_{term.}} \cdot i_{RMS}^2
\end{aligned} \tag{8}
$$

TABLE III
SPECIFICATION AND MAIN COMPONENT LIST OF THE PROTOTYPE

Component	Manufacturer, Part number	Parameters
40V MOSFET	Infineon, IQE013N04LM6ATMA1	40V, 1.35 mΩ
C_{in} & C_{out} terminal capacitors	TDK, C3216X5R1V106K160	50V, 10$\mu F\times$ 14
C_{res} resonant capacitors	TDK, C3216X5R1V106K160	50V, 10$\mu F\times$7
Switching frequency	N/A	220 kHz
Resonant indutor	parasitic inductance, air core	21nH
Gate driver	Infineon 1EDN7550U	SOT23-6

where $R_{ds,ON}$ is the on-state channel resistance of the MOSFET used, R_{PCB} is the PCB trace resistance and f_{sw} is the switching frequency. Q_{oss} represents the energy-equivalent junction charge of the MOSFET. N_{res} and $N_{term.}$ are the number of paralleled capacitors in resonant tank and terminals, respectively. The RMS current flowing through the resonant tank is bound by:

$$
i_{RMS} = \frac{\pi}{2\sqrt{2}} \cdot I_0 \tag{9}
$$

In the experiment, the converter was immersed in a silicon oil tank with a circulating pump to stabilize the ambient temperature of the CUTs. The load current was then swept from 2A to 36A, and the readings from a Yokogawa WT5000 power analyzer were used to plot the efficiency curve.

It should be noted that all SE coefficients used in equations (7) and (8) are dependent on the bias voltage, as demonstrated in Figure 20. The C3216X5R1V106K160 MLCC was used in the RSC converter, and its dielectric thickness t has been extracted by the DTO and is listed in Table A1. Feeding (7), where the ESR of C3216X5R1V106K160 is depicted, to (8) will generate the total loss of the RSC converter at various load conditions. Fig. 26 then plots the efficiency curves and illustrates a satisfying consistency between the calculated and measured efficiencies. This consistency demonstrates the accuracy and effectiveness of the proposed loss model in real converter applications. However, relying on the ESR from the datasheet can lead to a significant underestimation of Class II MLCC power loss.

Furthermore, Fig. 26 also provides a breakdown of the converter loss at four different load conditions. As shown, the contribution from MLCC loss is negligible at light load but increases to 21% of the total loss at maximum power, which is a substantial amount of loss compared to MOSFET's ohmic loss. In summary, the proposed loss model has been validated at both the device and converter levels. Device-level validation

confirmed that the model accurately estimates the losses of MLCCs with different materials, packages, capacitances, and bias voltages. Converter-level validation demonstrated the accuracy of the model in predicting the power losses of MLCCs in a resonant converter. These results validate the effectiveness of the proposed model, and provide a reliable tool for engineers to optimize power converter design by predicting the losses of MLCCs.

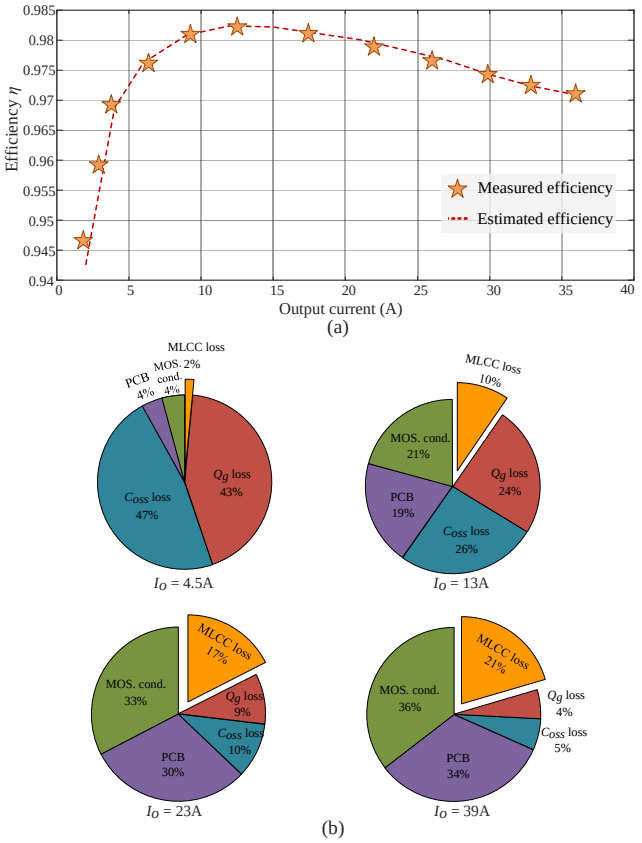


Fig. 26. (a) Comparison between measured and estimated efficiency curves, and (b) Loss breakdown of the prototype at four different load conditions.

VII. Conclusion

This paper presents a novel methodology for characterizing and modeling the loss behavior of Class II MLCCs, specifically focusing on the influence of high frequencies (>100 kHz) and DC bias voltage. The proposed methodology aims to offer a simple yet accurate toolkit for loss estimation in Class II MLCCs. It consists of several key components: a Res-ST testing circuit that functions as the excitation and characterization circuit, a microscope investigation that builds up material-specific loss information, a SPeG derived from the analogy between magnetic and dielectric material material to generalize the material-level information to devices, and a DTO that estimates the internal microstructural geometry with minimal destructive analysis, thus extending the SPeG to all devices utilizing the same material.

The primary contribution of this work is an accurate reveal of the influence of various intertwined factors, such as frequency, excitation level, and DC bias, on the loss behavior of ferroelectric dielectric materials. Additionally, our experimental results uncover the coexistence of both bias-sensitive, where loss increases with higher bias voltage, and bias-insensitive Class II dielectric materials. This finding resolves the conflicts present in previous literature [2], [9].

The accuracy of the proposed loss model has been validated on devices using various materials, and an illustrative example has been provided to demonstrate the implementation of the loss model on an actual resonant converter. It is anticipated that these developed loss characterization and modeling techniques will facilitate the estimation of losses in Class II MLCCs, making it as straightforward as estimating losses in common magnetic devices.

Acknowledgement

The authors would like to thank Dr. David Menzi from ETH Zurich for his valuable suggestions on the calibration of the measurement circuit and loss modeling under DC bias.

Appendix

Understanding and mitigating measurement error is a crucial step to ensure the accuracy and validity of the loss characterization circuit. This appendix describes the procedures for deskewing and calibrating the proposed Res-ST circuit. Additionally, it presents the estimation performance of the proposed DTO on different types of dielectric materials.

A. Calibration of the Proposed Res-ST Circuit

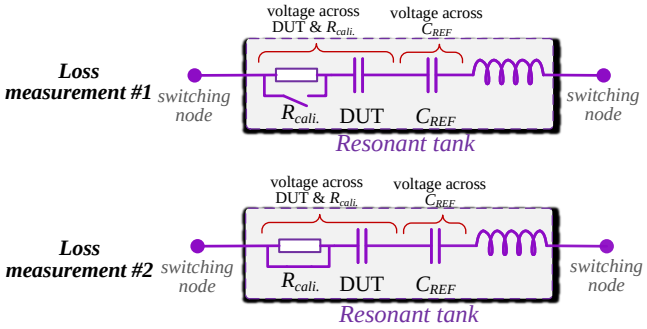


Fig. 27. Schematic of calibration circuit for the proposed Res-ST circuit.

To calibrate the accuracy of the test setup, we developed an electrical calibration method called differential power calibration. In this method, a shunt resistor ($R_{cali.}$) is placed in close proximity to the CUT, and two identical measurements are conducted sequentially, as shown in Fig. 27, with the only difference being the inclusion of the shunt resistor. By subtracting the loss obtained in measurement #2 from that obtained in measurement #1, and converting the differential power back to the ESR, the resulting ESR should match the nominal resistance of $R_{cali.}$. The difference between ESR calculated using the differential power and the nominal resistance of $R_{cali.}$ serves as an index of the accuracy of the measurement setup.

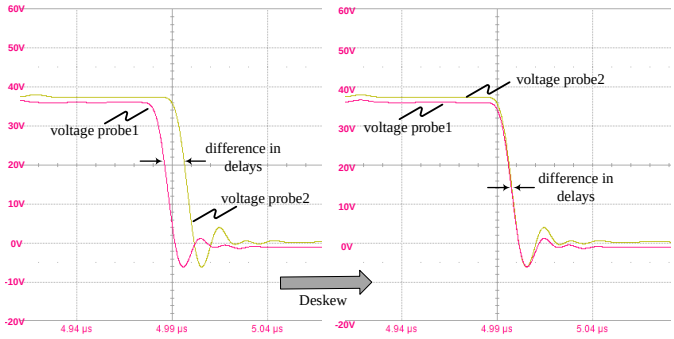


Fig. 28. Waveforms of the voltage probes before deskew (left) and after deskew. (right)

B. Deskew of Differential Probes

(1) Deskew via high steepness voltage edge:

The Res-ST circuit's current-source driving capability comes with a floating test ground, which may introduce measurement inaccuracies. To address this, multiple measures have been implemented. As seen in Fig. 4. (c), the measurement board is integrated with a half-bridge with a low loop inductance design, resulting in a high dv/dt voltage edge. Prior to the test, two differential probes with the same model (HVD3106A) are both connected across the switching node and the ground of the half-bridge to calibrate and compensate for the delay time in the oscilloscope. The adjustment process for the delay time of two probes, which aims to ensure proper alignment, has been depicted in Fig. 28.

(2) Suppression of common-mode (CM) noise:

The Res-ST is a measurement circuit that utilizes differential voltage probes in a floating-ground configuration. In this context, it is important to consider the effects of the alternating common-mode (CM) voltage that may impact the accuracy of the measurements. Among the various components of the CM voltage seen from the differential probe, the fast slew rate (dv/dt) of voltage at the switching node is of particular concern due to the high frequency components contained in the switching voltage transient. This can be problematic since it falls within the low common-mode rejection ratio (CMRR) range of the probe. However, in the test circuit, the output voltage (V_o), which determines the amplitude of the dv/dt transients, is set to a low value (<2V in all measurements in this work) due to the current-source nature of the driving circuit. Additionally, since both half-bridges operate in zero-current switching, the dv/dt from the switching edge is considerably low (<0.4V/ns). These measures help mitigate potential high-frequency CM noise from the source.

Fig. 7 shows the experimental waveforms, which demonstrate that the output voltage consistently maintains a low value (<2V) throughout the measurement process, ensuring that the amplitude of the high-frequency CM voltage is low. For benchmarking purposes, a pair of optically isolated probes with high CM noise immunity, IsoVu: TIVH08 from Tektronix, were used, and no differences were observed in the power loss results. However, as one of the motivations of this work is to develop a cost-effective test solution, the conventional HVD3106A differential probes were used for the rest of the test.

C. Estimation Accuracy of the Proposed DTO on Four Types of Dielectric Materials

TABLE A1
ESTIMATION ACCURACY OF THE DTO ON X5R-LV SAMPLES

Part number	t under SEM(μm)	$\widehat{t}$ under DTO(VNA) (μm)	error	$\widehat{t}$ under DTO(DS) (μm)	error
C2012X5R1C225K125	2.51	2.44	-2.8%	2.53	+0.9%
C2012X5R1E225K125	2.5	2.46	-1.6%	2.55	+1.9%
C2012X5R1V225K125	4.0	4.06	+1.6%	3.84	-4.1%
C2012X5R1H225K125	3.94	4.07	+3.2%	4.22	+7.1%
C2012X5R1C475K125	2.08	2.15	+3.4%	2.27	+9.1%
C2012X5R1E475K125	2.58	2.59	+0.3%	2.82	+8.8%
C2012X5R1H475K125	2.59	2.58	-0.1%	2.79	+7.7%
C3216X5R1E106K160	2.85	2.79	-2.1%	3.05	+7.0%
C3216X5R1V106K160	3.17	3.16	-0.3%	3.22	+1.6%
C3216X5R1H106K160	2.95	3.16	+7.1%	3.25	+10%

TABLE A2
ESTIMATION ACCURACY OF THE DTO ON X7R-LV SAMPLES

Part Number	t under SEM (μm)	$\widehat{t}$ from DTO (μm)	error
C2012X7R1E475K125	3.18	3.10	-2.5%
C2012X7R1V475K125	3.29	3.09	-5.8%
C3216X7R1V475K160	4.58	4.75	+3.6%
C3216X7R1V225K160	7.25	7.35	+1.4%
C3216X7R1E106K160	3.47	3.35	-3.7%
C3216X7R1C106K160	2.85	2.80	-1.8%
C2012X7R1E225K125	4.88	4.88	+0.0%
C2012X7R1H225K125	4.88	4.86	-0.4%
C2012X5R1V225K125	4.88	4.87	-0.2%

TABLE A3
ESTIMATION ACCURACY OF THE DTO ON X7T-HV SAMPLES

Part number	t under SEM (μm)	$\widehat{t}$ from DTO (μm)	error
C3216X7T2E224K160	10.37	10.00	-3.5%
C4532X7T2E105K250	10.37	10.66	+2.8%
C4532X7T2W474K230	17.69	17.28	-2.3%
C4532X7T2J224K200	22.86	22.88	+0.1%
C5750X7T2J474K250	22.60	23.37	+3.4%
C5750X7T2W105K250	16.45	15.37	-6.5%

TABLE A4
ESTIMATION ACCURACY OF THE DTO ON X7R-HV SAMPLES

Part number	t under SEM (μm)	$\widehat{t}$ from DTO (μm)	error
C5750X7R2J224L230	48.0	49.4	+2.9%
C4532X7R2K104L230	48.0	46.83	-2.4%
C4532X7R2E474K230	23.0	22.27	-3.1%
C3225X7R2E224K200	23.0	21.93	-4.6%
C5750X7R2E105K230	22.2	21.5	-3.2%
C3216X7R2A105K160	8.9	8.58	-3.6%
C3225X7R2A225K230	8.88	9.18	+3.4%

REFERENCES

[1] D. Cittanti, F. Stella, E. Vico, C. Liu, J. Shen, G. Xiu, and R. Bojoi, "Analysis and design of a high power density full-ceramic 900 v dc-link capacitor for a 550 kva electric vehicle drive inverter," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, 2022, pp. 1144–1151.

[2] D. Menzi, D. Bortis, G. Zulauf, M. Heller, and J. W. Kolar, "Novel igse-c loss modeling of x7r ceramic capacitors," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 367–13 383, 2020.

[3] M. Wei, Y. Li, Z. Ni, C. Liu, and D. Cao, "Zero voltage switching switched-tank modular converter for data center application," in *2019 IEEE 7th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*. IEEE, 2019, pp. 245–250.

[4] J. Xu, L. Gu, and J. Rivas-Davila, "Effect of class 2 ceramic capacitor variations on switched-capacitor and resonant switched-capacitor converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2268–2275, 2019.

[5] C. Rainer, R. Rizzolatti, and D. Varajao, "High density cascaded zvs switched capacitor converter for 48-v data-center application," in *PCIM Europe digital days 2020; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2020, pp. 1–8.

[6] N. Ellis and R. Amirtharajah, "A resonant 1: 5 cockcroft-walton converter utilizing gan fet switches with n-phase and split-phase clocking," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2020, pp. 19–25.

[7] S. Ben-Yaakov, "Some observations on loss and hysteresis of ferroelectric-based ceramic capacitors," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9127–9129, 2018.

[8] D. Menzi, M. Heller, and J. W. Kolar, "igse-c-a new normalized steinmetz model for class ii multilayer ceramic capacitors," *IEEE Open Journal of Power Electronics*, vol. 2, pp. 138–144, 2021.

[9] S. Coday and R. C. Pilawa-Podgurski, "High accuracy calorimetric measurements and modeling of ceramic capacitor losses under large ripple operation," in *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2020, pp. 188–194.

[10] I. Novak, "Dc and ac bias dependence of capacitors including temperature dependence," *DesignCon East*, 2011.

[11] C. B. Barth, T. Foulkes, I. Moon, Y. Lei, S. Qin, and R. C. Pilawa-Podgurski, "Experimental evaluation of capacitors for power buffering in single-phase power converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 8, pp. 7887–7899, 2018.

[12] M. Vasic, J. A. Oliver, P. Alou, J. A. Cobos, and P. J. Grbovic, "Experimental evaluation of capacitors for high power resonant converters," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2017, pp. 1–6.

[13] G. Zulauf, S. Park, W. Liang, K. N. Surakitbovorn, and J. Rivas-Davila, "Coss losses in 600 v gan power semiconductors in soft-switched, high-and very-high-frequency power converters," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 748–10 763, 2018.

[14] M. S. Nikoo, A. Jafari, N. Perera, and E. Matioli, "Measurement of large-signal c oss and c oss losses of transistors based on nonlinear resonance," *IEEE Transactions on Power Electronics*, vol. 35, no. 3, pp. 2242–2246, 2019.

[15] Y. Jiang, B. Hu, B. Wen, Y. Shen, and T. Long, "Methodology for large-signal loss characterization of ferroelectric class ii mlcc in high-frequency range," in *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2022, pp. 1–6.

[16] A. Teverovsky, "Cracking problems in low-voltage chip ceramic capacitors," Tech. Rep., 2019.

[17] T. Trzepiecinski and M. Gromada, "Characterization of mechanical properties of barium titanate ceramics with different grain sizes," *Materials Science-Poland*, vol. 36, no. 1, pp. 151–156, 2018.

[18] Y. Shen, H. Wang, Z. Shen, Y. Yang, and F. Blaabjerg, "A 1-mhz series resonant dc–dc converter with a dual-mode rectifier for pv microinverters," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6544–6564, 2018.

[19] Z. Ni, Y. Li, C. Liu, M. Wei, and D. Cao, "Development of a 100 kw sic switched tank converter for automotive applications," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*. IEEE, 2019, pp. 5848–5855.

[20] C. Jiang, X. Li, S. S. Ghosh, H. Zhao, Y. Shen, and T. Long, "Nanocrystalline powder cores for high-power high-frequency power electronics applications," *IEEE Transactions on Power Electronics*, vol. 35, no. 10, pp. 10 821–10 830, 2020.

[21] D. S. Specification, "Jedec standard," 2009.

[22] J. Muhlethaler, J. Biela, J. W. Kolar, and A. Ecklebe, "Core losses under the dc bias condition based on steinmetz parameters," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 953–963, 2011.

[23] X. Li, C. Jiang, H. Zhao, B. Wen, Y. Jiang, and T. Long, "Novel flexible nanocrystalline flake ribbons for high-frequency transformer design," in *2021 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2021, pp. 2891–2896.

[24] D. Neumayr, D. Bortis, J. W. Kolar, M. Koini, and J. Konrad, "Comprehensive large-signal performance analysis of ceramic capacitors for power pulsation buffers," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*. IEEE, 2016, pp. 1–8.

[25] G. Yang, Z. Yue, J. Zhao, H. Wen, X. Wang, and L. Li, "Dielectric behaviour of batio3-based ceramic multilayer capacitors under high dc bias field," *Journal of Physics D: Applied Physics*, vol. 39, no. 16, p. 3702, 2006.

[26] R. Placeres-Jiménez, J. Rino, and J. Eiras, "Modeling ferroelectric permittivity dependence on electric field and estimation of the intrinsic and extrinsic contributions," *Journal of Physics D: Applied Physics*, vol. 48, no. 3, p. 035304, 2015.

[27] F. Hämmerle and S. Sandler, "DC biased impedance measurements Capacitors-Capacitors," Tech. Rep., 2017.

[28] S. Sandler and P. Picotest, "An accurate method for measuring capacitor esl," *How2Power Today*, 2011.

[29] S. Jiang, S. Saggini, C. Nan, X. Li, C. Chung, and M. Yazdani, "Switched tank converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5048–5062, 2018.

[30] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor dc–dc converters," *IEEE transactions on power electronics*, vol. 23, no. 2, pp. 841–851, 2008.

[31] S. Ben-Yaakov. Modeling ceramic capacitors loss under high dc bias voltage and high current stress. Youtube. [Online]. Available: https://www.youtube.com/watch?v=d00FQxDmWCI

[32] Y. Zhu, Z. Ye, and R. C. Pilawa-Podgurski, "Modeling and analysis of resonant switched-capacitor converters with finite terminal capacitances," in *2021 IEEE 22nd Workshop on Control and Modelling of Power Electronics (COMPEL)*. IEEE, 2021, pp. 1–6.

Yunlei Jiang (S'14, M'23) received the B.Eng. degree from Nanjing Normal University, Nanjing, China, in 2015, the M.Sc. degree from Southeast University, Nanjing, China, in 2018, and the Ph.D. degree under the support of Jardine-Cambridge Scholarship from the University of Cambridge, Cambridge, U.K., in 2023.

He is currently a Senior Power Electronics Engineer(Starship) with SpaceX, Hawthorne, CA, US. From 2018 to 2019, he was a Research Assistant with WEMPEC, University of Wisconsin Madison, Madison, WI, USA. In 2022, he was a power electronics intern with the drive inverter team of Tesla Motor, Palo Alto, CA, US. His current research interests include high-reliability packaging, thermal design, and system integration of power electronics.

Borong Hu (M'21) received the B.Eng. degree in Electrical Engineering from Chongqing University, China, in 2014, and the Ph.D. degree in Power Electronics from the University of Warwick, UK, in 2021.

He is currently a Postdoctoral Research Associate with the University of Cambridge, UK. His research interests include the packaging integration, reliability, and condition monitoring of power electronics.

Yanfeng Shen (S'16, M'18) received the B.Eng. degree in electrical engineering and automation and the M.Sc. degree in power electronics from Yanshan University, Qinhuangdao, China, in 2012 and 2015, respectively, and the Ph.D. degree in power electronics from Aalborg University, Aalborg, Denmark, in 2018.

He is currently a Research Engineer in Power Electronic at Danfoss Silicon Power, Munich, Germany. From 2019 to 2021, he worked as a Postdoctoral Research Associate at the University of Cambridge, UK. He worked as an Intern with ABB Corporate Research Center, Beijing, China, in 2015. He was a Visiting Graduate Research Assistant with Khalifa University, UAE, in 2016. His current research interests include SiC MOSFET power modules, electric vehicle traction inverters, and power electronics reliability. Dr. Shen serves as an Industry Editor for the IET Renewable Power Generation.

Xufu Ren (S'19) received the B.Eng. degree in electrical engineering from Xian Jiaotong University, Xi'an, China, in 2019, and the M.Sc. degree in electrical engineering from Zhejiang University, Hangzhou, China, in 2022. He is currently working toward the Ph.D. degree with the University of Cambridge, Cambridge, UK. His research interests include high-efficiency and high-density dc-dc converters and magnetics.

Steve Sandler has been involved with power system engineering for more than 40 years. He is the founder and CEO of Picotest, a company specializing in instruments and accessories for high-performance power system and distributed system testing, as well as the founder of AEi Systems, a company specializing in modeling, simulation and analysis of large spacecraft. He frequently lectures at IEEE conferences and has published numerous articles and books on power electronics and power integrity related topics.

Stephan Hofmann is Professor of Nanotechnology at the Department of Engineering at Cambridge University, and Director of the EPSRC Doctoral Training Centre in Nanoscience and technology. He graduated in Physics at the Technische Universitat Munchen and obtained his Ph.D. at the University of Cambridge. Prior to his faculty position, he held a Dorothy Hodgkin Fellowship by the Royal Society and a Research Fellowship at Peterhouse, Cambridge, where he is currently a Bye-Fellow.

His research focuses on the application driven exploration of new device materials, bridging from fundamental discovery and characterisation of properties to functional device integration and manufacturing pathways. He has (co-)authored more than 250 journal papers in this field.

Teng Long (M'13) received the B.Eng. degree from the Huazhong University of Science and Technology, China, the first class B.Eng. (Hons.) degree from the University of Birmingham, UK in 2009, and the Ph.D. degree from the University of Cambridge, UK in 2013. Until 2016, he was a Power Electronics Engineer with the General Electric (GE) Power Conversion business in Rugby, UK.

He is currently a Full Professor with the University of Cambridge. His research interests include power electronics, electrical machines, and machine drives. Dr Long is a Chartered Engineer (CEng) registered with the Engineering Council in the UK.