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High-Throughput Electrical Characterization of Nanomaterials from Room to Cryogenic Temperatures

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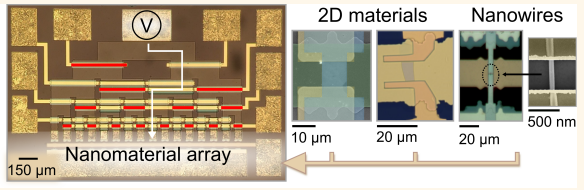
ABSTRACT: We present multiplexer methodology and hardware for nanoelectronic device characterization. This high-throughput and scalable approach to testing large arrays of nanodevices operates from room temperature to milli-Kelvin temperatures and is universally compatible with different materials and integration techniques. We demonstrate the applicability of our approach on two archetypal nanomaterials—graphene and semiconductor nanowires—integrated with a GaAs-based multiplexer using wet or dry transfer methods. A graphene film grown by chemical vapor deposition is transferred and patterned into an array of individual devices, achieving 94% yield. Device performance is evaluated using data fitting methods to obtain electrical transport metrics, showing mobilities comparable to nonmultiplexed devices fabricated on oxide substrates using wet transfer techniques. Separate arrays of indium-arsenide nanowires and micromechanically exfoliated monolayer graphene flakes are transferred using pick-and-place techniques. For the nanowire array mean values for mobility μ_{FE} = 880/3180 cm^2 V^{-1} s^{-1} (lower/upper bound), subthreshold swing 430 mV dec^{-1}, and on/off ratio 3.1 decades are extracted, similar to nonmultiplexed devices. In another array, eight mechanically exfoliated graphene flakes are transferred using techniques compatible with fabrication of two-dimensional superlattices, with 75% yield. Our results are a proof-of-concept demonstration of a versatile platform for scalable fabrication and cryogenic characterization of nanomaterial device arrays, which is compatible with a broad range of nanomaterials, transfer techniques, and device integration strategies from the forefront of quantum technology research.



KEYWORDS: *nanoelectronic device arrays, scalable fabrication, high-throughput testing, graphene and 2D materials, nanowires, electronic characterization*

For technologies to be realized from the many intriguing nanomaterial devices that are being developed in research laboratories, it is essential to have scalable approaches[1] that lean toward mass production, measuring device repeatability, and optimizing designs. We present a high-throughput testing technique for electrical characterization of nanotechnology device arrays. In this work, its specific applicability to 2D materials and nanowires and compatibility with different material fabrication/transfer schemes are demonstrated. The variability of nanoscale electronic device performance is a significant issue for the fabrication of complex circuit designs, particularly those that rely on quantum phenomenon and require mounting and cooling in cryogenic systems. Devices are tested individually, and multiple repetitions must be fabricated and measured to find working examples. This is time-consuming, and samples cannot be later integrated into circuit designs if they perform well. By introducing a multiplexer system, many devices can be tested in a single experimental run.

We study arrays of devices from graphene grown by chemical vapor deposition (CVD), mechanically exfoliated graphene devices, and InAs nanowire devices. The CVD graphene is wet transferred as a continuous 2D material film, and exfoliated

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flakes and nanowires are transferred by pick-and-place techniques. Each device is individually measured using a multiplexing technique that can operate from room to milli-Kelvin temperatures. This scheme requires no modification of current experimental apparatus, which can be costly and time-consuming, does not suffer from carrier freeze-out, which can render commercial alternatives inoperative, and is capable of operating at high magnetic fields. The multiplexer and array are integrated on a single chip of similar size to chips used for nonmultiplexed devices and does not require integration or testing of off-the-shelf components.

Beyond 2D materials and nanowires, cases where this technique might be beneficially applied for statistical analysis and high-throughput testing include arrays of inkjet-printed transistor circuits,[2−4] molecular transistor arrays created by plating colloidal particles in nanogaps,[5,6] transistor arrays such as carbon nanotubes deposited using electrophoresis techniques,[7] molecules in graphene nanogaps,[8,9] and possibly even biological applications such as multiplexing DNA microarrays.[10] The multiplexer will also enable studies such as investigating the role of damage/disorder and modification of device properties[11,12] by varying the amount of irradiation across the array, for example using a focused ion beam, or comparing ensemble averaging with single-device averaging techniques used to study phase coherent properties in 2D graphene,[13,14] graphene nanoribbons,[15] and nanowires.[16−20]

The GaAs heterostructure is capable of operating over a wide temperature range, allowing prechecking at room temperature before testing of devices in cryogenic conditions where quantum effects are exploited for quantum technology and functional electronics. Since exotic phenomena in quantum research are often only found in the best of a batch of devices, scaling up measurement will speed up this search and provide large-scale statistics of how reproducible phenomena are.[21−24] Device geometries can be varied across the array to systematically assess impact on performance[25] and optimize designs. Multiplexing can also be used to reveal relationships between the physical and electrical parameters, as seen in arrays of split gate transistors.[26] Additionally, there is the possibility of one or two devices in the array possessing unique properties, *e.g.*, due to being the narrowest or shortest in a distribution of dimensions, which allows opportunistic study of unusual phenomena. So far, the multiplexer has been used for devices fabricated within the two-dimensional electron gas (2DEG) itself,[21,25−27] limiting its applicability. Here, we take the approach of integrating arbitrary nanomaterials using transfer techniques, which allows the platform to be used to study different materials and physics.

Arrays contain $2^{(t-3)/2}$ devices, where t is the total number of electrical contacts, including input, output, addressing gates, and back gate for local density control. Arrays of up to 16 devices are measured as a proof-of-principle, requiring 11 contacts. Very few additional contacts are required to measure much larger arrays; for example 19 or 21 contacts are needed for 256 or 512 devices, respectively. In the following sections the multiplexer operation is described, followed by a demonstration of room-temperature addressing. The results are organized in two categories, multiplexing arrays fabricated from large-area 2D materials (for which we test CVD-grown monolayer graphene) or pick-and-place techniques (for which InAs nanowires and mechanically exfoliated monolayer graphene flakes are tested).

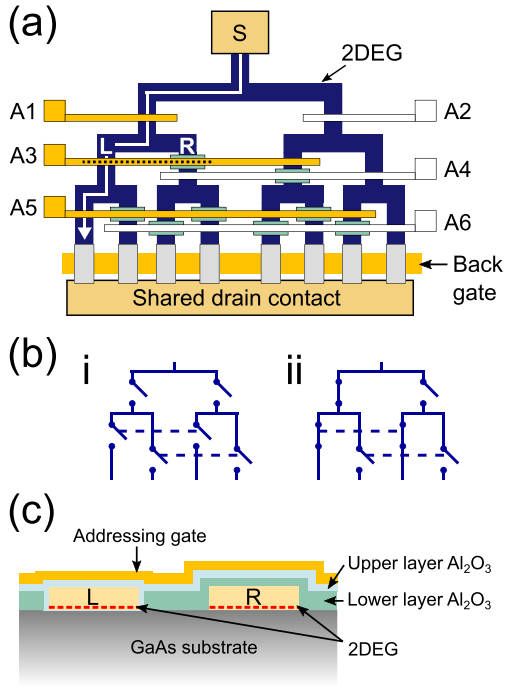

Figure 1. (a) Schematic diagram of a multiplexer with one source input (S) connected to eight output channels. Addressing gates are labeled A1 to A6. In this example channel 1 is selected by applying voltages to several addressing gates. White (yellow) gates indicate a voltage is (is not) applied. The white arrow shows the current path through the multiplexer. Insulated regions depicted by green rectangles below the gates, such as at 'R', prevent depletion of the 2DEG when addressing gates are biased. Gray rectangles show the location of nanomaterials at the multiplexer output, one per channel, connected to a common drain output. (b) Equivalent circuit of the top two levels of the multiplexer. Dashed lines indicate switches that are controlled by the same addressing gate. All switches are open in (i), corresponding to addressing voltages applied to all gates. Certain switches are closed in (ii) to address channel 1. (c) Cross section through two branches of the multiplexer, corresponding to the dotted line in (a). For all multiplexers in this study the branches corresponding to 'R' are covered by a layer of Al_2O_3. A thinner upper layer covers both branches for the multiplexed CVD graphene array.

RESULTS AND DISCUSSION

A single multiplexer design is used throughout this study. A schematic layout with eight channels is shown in Figure 1(a). The conduction path is defined in a 2DEG of a GaAs heterostructure. Multiplexer outputs are selected using addressing gates, labeled A1 to A6. A negative voltage is applied to half the addressing gates, depleting the 2DEG below. White (yellow) represents when a depletion voltage is (is not) applied. In this example voltages are applied to A2, A4, and A6, to select the left-most channel. In certain locations the addressing gates cross channels that must remain open when an addressing voltage is applied. An additional insulating layer is added beneath the gate at these points to prevent the 2DEG depleting. A back gate is defined adjacent to multiplexer outputs and covered with Al_2O_3 deposited by atomic layer deposition (ALD). Nanomaterials are transferred on top of the insulator and connected *via* source/drain electrodes to multiplexer outputs and the common drain. The location of the nanomaterials is indicated by the gray rectangles in Figure 1(a).

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Figure 1(b) shows an equivalent circuit of the top two multiplexer levels. In (i) all switches are open, corresponding to a depletion voltage applied to all addressing gates. In (ii) the voltage on several gates is set to zero (the switches are closed), to select channel 1. Figure 1(c) shows a cross section through two adjacent arms of the multiplexer, as along the black dotted line in Figure 1(a). All multiplexers are covered with an Al_2O_3 layer deposited by ALD, which is removed over specific channels by HF etching. This creates a voltage range where the 2DEG can be depleted wherever the lower layer has been removed, such as at L, but not at R [Figure 1(c)]. The multiplexer used for CVD graphene also has a second, thinner layer of Al_2O_3 covering both channels, to prevent current leaking from surface gates to the GaAs at room temperature. Figure 2(e) shows the 16-channel multiplexer fabricated for this study. The branching structure outlines the etched mesa containing the 2DEG. Ohmic contacts are defined at the multiplexer source and at each output (labeled 1 → 16).

Room-Temperature Operation. To demonstrate addressing gate functionality, Figure 2(a) and (b) show conductance G as a function of addressing gate voltage $V_{A,i}$ at room temperature and T = 4.2 K, respectively, where i is the addressing gate index. A multiplexed array of CVD graphene is used in this example, with lower and upper Al_2O_3 gate dielectric thicknesses of ∼110 and ∼15 nm, respectively (the total gate oxide thickness under the CVD graphene ≈ 125 nm). The number of working devices can therefore be determined prior to cool down. The differential conductance is measured using a two-terminal constant source−drain voltage V_{sd} at 77 Hz, typically V_{sd} = 100 μV. Measurements at T = 4.2 K are performed with the sample immersed in liquid helium. Addressing gates A5 (black trace) and A6 (red trace) are swept in the negative direction consecutively. The 2DEG is first depleted beneath A5 (blocking half the channels), then beneath A6 (blocking the remainder); $V_{A,i}$ = 0 V for all other gates. The behavior is the same at room temperature and T = 4.2 K, aside from changes in depletion voltage and overall conductance. Figure 2(c) and (d) show examples of addressing a specific channel (channel 9) at room temperature and T = 4.2 K, respectively. The current path is illustrated pictorially in Figure 2(e), where red bars indicate depletion of the 2DEG.

The current ratio as addressing gates are swept [Figure 2(c) and (d)] is governed by the resistance of each channel, which includes the 2DEG, device, and contact resistance. The 2DEG resistance can be estimated for each channel by considering the area in terms of the aggregated length-to-width aspect ratio $N = L/W$ and calculating sheet resistance $R = L/\sigma W$ where $\sigma = ne\mu$. For the device measured in Figure 2, the 2DEG sheet density and electron mobility are measured on a separate Hall bar device as $n = 1.53 \times 10^{11}$ cm^{-2} and $\mu = 8.17 \times 10^5$ cm^2 V^{-1} s^{-1}, respectively. Here N = 10 for channels 1, 2, 15, and 16, N = 9 for channels 3, 4, 7, 8, 9, 10, 13, and 14, and N = 8 for channels 5, 6, 11, and 12, corresponding to R = 500, 450, and 400 Ω, respectively. The maximum path-dependent difference in 2DEG resistance (≈100 Ω) is much smaller than variations in contact resistance for the arrays measured here (on the order at least kΩ); therefore device variability is the largest factor determining the current ratio.

CVD-Grown Graphene. Monolayer graphene films are grown by CVD on Cu and transferred to the multiplexer by etching the Cu in a $(NH_4)_2S_2O_8$ solution with poly(methyl methacrylate) (PMMA) protection of graphene.[28] Source and drain electrodes (Ti/Au) are created prior to transfer, Figure 3(a). Graphene channels 10 μm wide are defined at outputs of

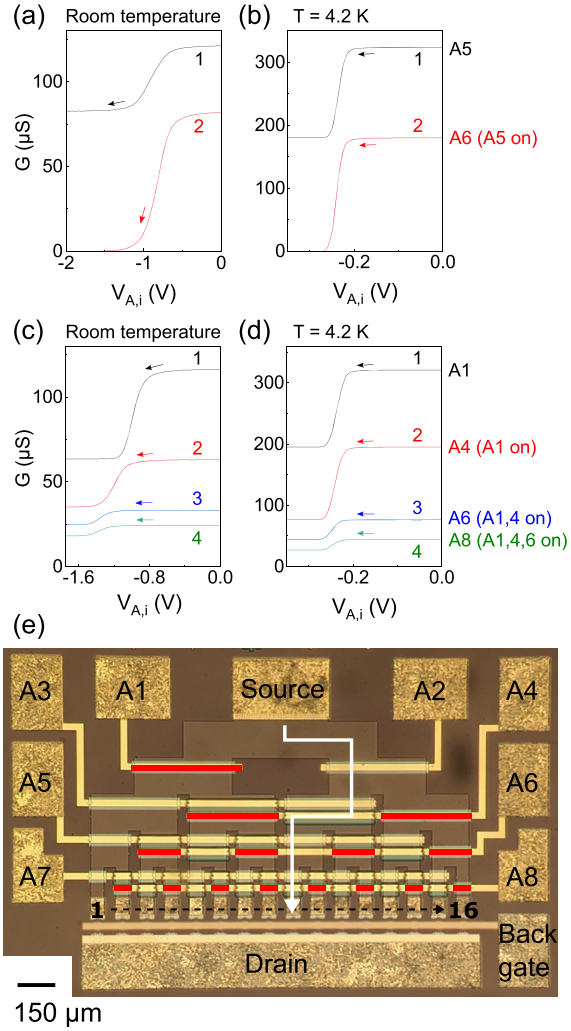

Figure 2. Room-temperature and T = 4.2 K operation. (a and b) Source−drain conductance as a function of addressing gate voltage $V_{A,i}$, where i is the gate index. Gates A5 (black trace) and A6 (red trace) are swept sequentially as indicated by labels 1 and 2, with $V_{A,i}$ = 0 V for all other gates. The voltage is maintained on A5 while A6 is swept (*i.e.*, the gate is "on"). Each multiplexer output is connected to a single graphene device, all of which share a common drain contact. (c and d) Addressing channel 9 at room temperature and T = 4.2 K, respectively. Gates A1, A4, A6, and A8 are swept sequentially as indicated by labels 1 to 4, and voltages are maintained on each gate after sweeping. Channel 9 addressing is illustrated on the multiplexer in (e), where the white arrow indicates the current path. Gates A1, A4, A6, and A8 deplete the 2DEG at the red bars. The lighter color branching structure indicates the mesa containing the 2DEG.

the multiplexer, and graphene is removed from unwanted areas by etching in an O_2 plasma. Source−drain contacts are separated by 10 μm. Further fabrication details are described in Methods. Figure 3(b) shows a false-color scanning electron microscope (SEM) image of a single graphene device. Blue, yellow, and green indicate graphene, source/drain contacts, and the back gate, respectively. Figure 3(c) shows a cross section from source to drain.

Measurements are performed in a ^{3}He cryostat with a base temperature of T = 0.28 K. Typical Dirac behavior is observed for 15 of 16 devices, corresponding to 94% yield (channel 11 did not conduct). This compares favorably to yields of more

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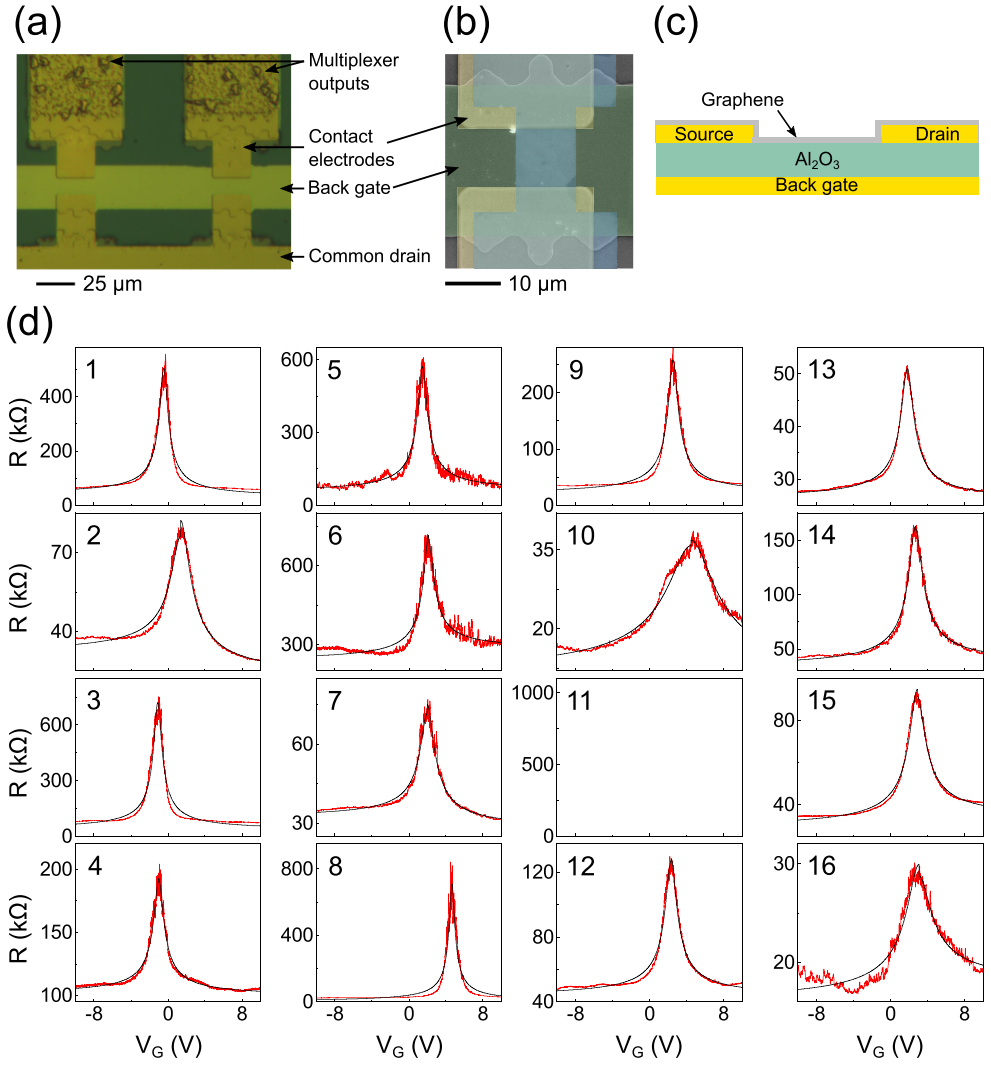

Figure 3. Multiplexed CVD graphene. (a) Two multiplexer outputs and drain contacts prior to graphene transfer. (b) False-color SEM of a single device. Green, yellow, and blue indicate the back gate, contact electrodes, and graphene, respectively. (c) Cross section through an individual device. (d) Transfer curves for each graphene device at T = 0.28 K. Black lines are fits to the data using eq 1. Channel numbers are given by each panel. Channel 11 did not conduct (G < 0.25 μS at all V_G).

industrially produced devices[29,30] and to multiplexed devices created within the 2DEG.[27] Figure 3(d) shows transfer curves for all devices. The two-terminal differential conductance is measured as a function of back gate voltage (V_G). The total device resistance is modeled using[31,32]

$$R_{Total} = R_P + L/(We\mu\sqrt{n_0^2 + n^2}) \quad (1)$$

where μ is the carrier mobility, n_0 is the residual carrier density, L and W are the length and width, respectively, n is the back-gate-dependent carrier density, and R_P is the total parasitic resistance. The carrier density is given by $n = C_G(V_G - V_{CNP})/e$, where V_{CNP} is the charge-neutrality-point voltage, C_G is the gate capacitance per unit area ($C_G = \epsilon_0\epsilon/d$), ϵ_0 is the free space permittivity, ϵ is the oxide permittivity, and d is the oxide thickness. Separate mobilities and parasitic resistances are estimated for electron and hole carriers such that $\mu = \mu_{hole}$ and $R_P = R_{P,hole}$ for $V < V_{CNP}$ and $\mu = \mu_{electron}$ and $R_P = R_{P,electron}$ for $V > V_{CNP}$. The V_{CNP} is found by first fitting with a single density-independent μ and R_P. Capacitance C_G is estimated using high magnetic field measurements performed on two example channels (13 and 14), Figure 4(a) and (b), discussed below, giving a mean $C_G \approx 34$ nF cm^{-2} from the gate dependence of the $\nu = \pm 2$ quantum Hall states, where ν is the filling factor, using $n = \nu eB/h$.

Estimated electronic parameters are listed in Table 1, where devices are categorized as "pristine" or "unique" according to

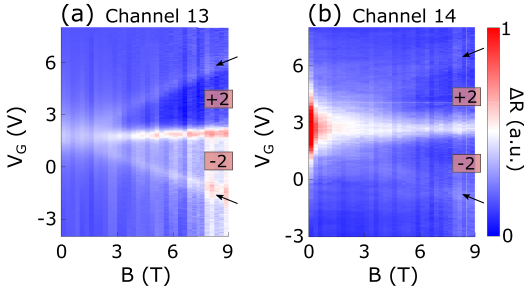

Figure 4. (a and b) Device resistance $\Delta R(V_G) = R(V_G) - R(8)$ as a function of V_G and magnetic field for channels 13 and 14, respectively. Labels ±2 refer to filling factors $\nu = \pm 2$, respectively. Arrows highlight the location and gradient of Landau levels −1 and +1.

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Table 1. Parasitic Resistances, Charge Neutrality Point (CNP) Voltage, Residual Carrier Density, and Mobilites Extracted from Fits to Transfer Curves in Figure 3(d) with Asymmetric Hole and Electron Mobilities and Parasitic Resistances[a]

channel	L/W	$R_{P,hole}$ (kΩ)	$R_{P,electron}$ (kΩ)	V_{CNP} (V)	n_0 ($\times 10^{11}$ cm^{-2})	μ_{hole} (cm^{2}V^{-1}s^{-1})	$\mu_{electron}$ (cm^{2}V^{-1}s^{-1})	l_{hole} (nm)	$l_{electron}$ (nm)
Pristine									
2	1	31.5	22.6	1.35	1.9	720	540	8.2	5
7	1	31.9	27.7	1.97	1.4	1110	930	11.9	8.8
9	1	19.2	20	2.55	1	260	270	3.4	2.8
12	1	43.1	42.9	2.32	1.2	640	630	7.6	6
14	1	33.3	36.7	2.71	1.4	350	360	3.6	3.7
15	1	28.9	33.6	2.9	1.6	590	670	6.3	6.9
16	1	16	17.9	3.08	2.5	1780	2270	16.8	19.9
mean		29.1	28.8	2.41	1.6	780	810	8.2	7.6
std		9.1	9.3	0.6	0.5	520	680	4.8	5.8
Unique									
1	1	40.5	28.1	−0.46	0.8	160	150	1.7	1.9
3	1	36.4	32	−1.11	0.8	110	110	1.3	1.4
4	1.17	100.9	99.3	−1.01	1	810	780	8.8	7.3
5	1	52.6	59.1	1.47	1	130	130	1.6	1.1
6	1.25	238.3	282.1	2.14	1.1	150	180	2.6	1
8	0.44	0	0	4.64	0.6	70	70	1.1	1
10	1	11.1	9.9	4.46	5	510	470	5.3	6
13	0.51	26.2	25.8	1.81	1.3	1030	1000	11	9.5
mean		63.2	67	1.49	1.4	370	360	4.2	3.6
std		77	92.2	2.27	1.4	370	350	3.8	3.4

[a]The mean free paths are estimated using eq 2 at n_{hole} and $n_{electron} = 6 \times 10^{11}$ cm^{-2}. Devices are categorized as pristine or unique depending on whether cracks/folds in the graphene or significant transfer residues are evident in SEM images.

whether μm scale process-induced defects or significant transfer residues are visible in SEM images, shown in Supporting Information. Eight devices are classified as unique, where imperfections include holes/gaps and whether graphene appears multilayer, folded, or larger than intended. The total parasitic resistance includes contact electrodes to the device under test (R_C), the multiplexer 2DEG, ohmic contacts, and circuit/cryostat wiring. It is likely that R_C is by far the dominant term, since separate measurements estimate that the multiplexer and wiring contribute an average of ∼469 Ω per channel, as discussed in Methods. Equation 1 overestimates R_P since it assumes the resistance at high density is only due to the contact resistance and does not take into account any other effects.[32] Therefore values in Table 1 are an upper bound. The model does not result in a good fit for channel 8, which appears in the SEM image to be a mixture of different parallel areas with varying thicknesses indicated by a varying contrast between areas of graphene[33] (Supporting Information). The device conductance is therefore a nontrivial addition of these areas, and attempting to fit the transfer curve—which shows a significant increase in resistance (35-fold from $V_G = -10$ V to the charge neutrality point)—leads to the unrealistic $R_P < 0.1$ Ω. For future devices improvements must be made to reduce contact resistance, since there is the possibility of interlayer contamination from the transfer process as source−drain electrodes connecting the graphene are fabricated prior to transfer. Nevertheless, the high device yield (15/16) and similarity of electronic parameters compared to nonmultiplexed devices illustrate the versatility and power of the multiplexed approach. The multiplexer is amenable to more sophisticated contacting methods which achieve lower contact resistance, such as using edge contacts,[34,35] fabricating contacts post-transfer, using electron-beam (e-beam) lithography to define graphene areas to avoid use of UV photoresists, cleaning contact areas using an oxygen plasma[36,37] or UV ozone[38] prior to metallization, or thermal annealing techniques.[37,39,40]

Data from pristine devices allow assessment of the variability in transport parameters across a single CVD graphene sheet. The estimated residual carrier densities are similar to values estimated for graphene grown by CVD on Ni[41] on Si/SiO_2 substrates and for exfoliated graphene.[31] The mobilities of pristine devices vary from 260 to 2270 cm^2 V^{-1} s^{-1} and are similar to values achieved for wet-transferred CVD graphene on an oxide substrate,[42] although separate high magnetic field measurements imply the mobility may be much higher than values estimated using eq 1, up to $\mu \approx 4000$ cm^2 V^{-1} s^{-1} for channel 13 (discussed below). The lowest mobilities occur for devices in the unique category, where cracks, residues, or debris may be responsible. Grain boundaries can lead to lower mobility due to preferential adsorption of residues which dope graphene and scatter carriers, although grain sizes for similar CVD graphene have been measured at >100 μm,[43] larger than our device area of 10×10 μm^2. Therefore, each device is not likely to contain more than one grain boundary, so these are unlikely to be a significant factor here. Another possibility is chemical adsorption from transfer residues and exposure to atmospheric conditions, which can be mitigated against by encapsulation of the graphene.[44−47] All pristine and most unique channels show positive V_{CNP}, indicating slight p doping. These factors may contribute to asymmetries of electron and hole characteristics, which arise from scattering from adsorbates,[48] as well as from metal-induced doping at the contacts[48−52] causing a pinning of the Fermi energy in the contacts at a different value from the channel.

A small hysteresis ($\Delta V_{CNP} = V_{CNP}(\text{down}) - V_{CNP}(\text{up})$) is observed between transfer curves for V_G swept in the up and down directions (data presented in Figure 3 and Table 1 are for V_G swept in the up direction). For pristine/unique devices the mean $\Delta V_{CNP} = 0.49/0.47$ V, corresponding to a carrier trap

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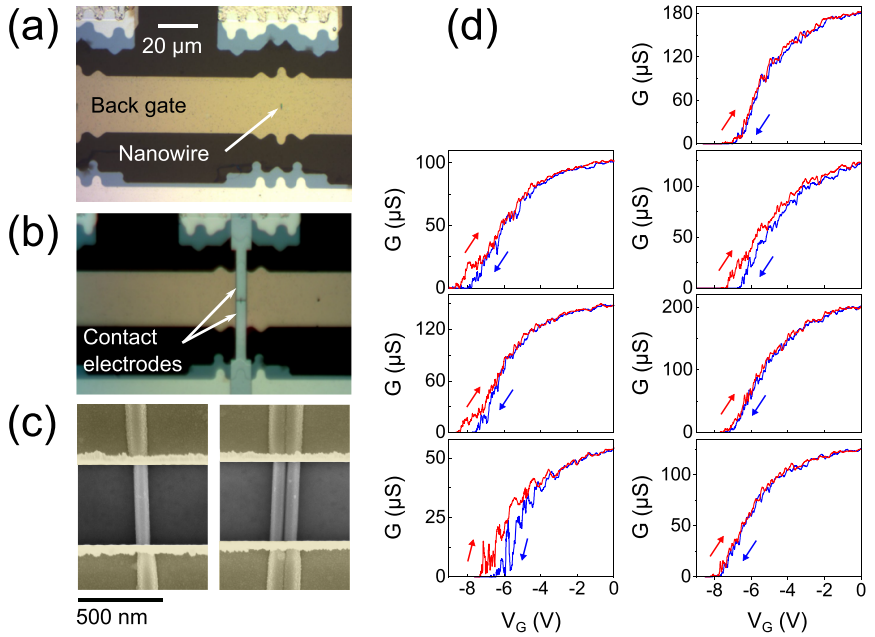

Figure 5. Multiplexed nanowire arrays. (a) Nanowires are placed at every multiplexer output, above a back gate covered with ≃50 nm thick Al_2O_3. (b) Top contacts defined by electron-beam lithography connect nanowires to multiplexer output channels and the common drain. (c) Scanning electron micrographs of an example single nanowire and nanowire pair in a multiplexed array. Contact electrodes are shown in false color (yellow). (d) Differential conductance as a function of back gate voltage for L = 401 nm (left column) and L = 606 nm (right column) nanowires, before subtraction of series and contact resistance. Red and blue arrows indicate the direction of the gate voltage sweep.

density[46] of $1.6/1.5 \times 10^{11}$ cm^{-2} using a capacitive model, $\Delta n = C_G \Delta V_{CNP}/e$. The gate voltage is swept slowly (dV_G/dt = 100 V h^{-1}), to estimate maximum hysteresis.[46]

Device mobilities can also be estimated from quantum Hall measurements. Compatibility of the multiplexer with magnetic field is important as it allows for magnetotransport measurements, which are a useful tool for probing physics in quantum devices. When the magnetic field is high enough, the 2D density of states becomes quantized in Landau levels[53,54] and electrons undergo cyclotron motion. Figure 4(a) and (b) show resistance, $\Delta R(V_G) = R(V_G) - R(8)$, as a function of V_G and magnetic field for channels 13 and 14, respectively, where $R(8)$ denotes the resistance at V_G = 8 V. This background resistance at high carrier concentration is subtracted at each B to improve the visibility of Landau levels. The darker areas indicate quantum Hall plateau regions with filling factors $\nu = \pm 2$. For channel 13, Landau level separation is visible for $B \gtrsim 2.25$ T. We use the approximation that $\tau \approx 1/\omega_c$ and $\mu \approx 1/B$ at the minimum B when Landau levels start to appear, since $\tau\omega_c \gg 1$ or $\mu B \gg 1$ is required for Landau levels to be clearly observed.[55] Here $\omega_c = v_F\sqrt{2eB/\hbar}$, τ is the scattering time, and v_F is the Fermi velocity. This corresponds to $\mu = 1/B$ = 4444 cm^2 V^{-1} s^{-1} and mean free path l = 12 nm using $l = v_F\tau$ and $v_F = 1 \times 10^6$ m s^{-1}. The gate capacitance is estimated using $dn/dB = \nu e/h$ for a capacitive model $en = C_G(V_G - V_{CNP})$, where V_{CNP} is the charge neutrality point voltage, giving $C_G \approx 37$ and 31 nF cm^{-2} for channels 13 and 14, respectively (for channel 14 Landau levels are less distinct, therefore this value is only approximate). A mean value of $C_G \approx 34$ nF cm^{-2} is used in our analysis.

Finally, we calculate the mean free path from device resistivity using the Drude model:

$$l = \frac{h}{2e^2\rho\sqrt{\pi n}} \quad (2)$$

where ρ is sheet resistivity $\rho = R(W/L)$, and R is the device resistance after correcting for series resistance. Mean free path values at n_{hole} and $n_{electron} = 6 \times 10^{11}$ cm^{-2} are given in Table 1 for each channel. For pristine devices, mean values of l = 8.2 and 7.6 nm are estimated for holes and electrons, respectively. Plots of l as a function of n are provided in Supporting Information. Uncertainties in these values may be introduced from the estimates of R_P and length-to-width ratio and for unique devices the assumption that each device is single-layer graphene. For comparison, a mean free path of nearly 40 nm at similar density is reported for CVD graphene wet transferred onto hexagonal boron nitride,[56] at T = 80 K.

We note that further studies such as testing reproducibility of electronic properties from cool down to cool down and performing magnetoresistance measurements are all possible with the multiplexer. A wide variety of 2D materials can be grown by CVD[57,58] and transferred in a similar way; therefore the method presented here makes it possible to study large arrays of devices from many different 2D materials.

Nanowires. Wurtzite (WZ) InAs nanowires are grown *via* metal organic vapor phase epitaxy using 50-nm-diameter Au nanoparticles to drive anisotropic nanowire growth. Growth is performed in an Aixtron 200/4 reactor using trimethylindium (1.2×10^{-5} mol/min) and arsine (3.3×10^{-5} mol/min) precursors at a growth temperature of 500 °C. Further growth details can be found in ref 59. Nanowires are spread on a donor substrate (PDMS) and individually transfer printed[60−63] to another location on the PDMS surface, to create a 1D array. Selected nanowires are then transfer printed on top of the ≃50-nm-thick Al_2O_3 oxide covering the back gate on the multiplexer, using a flat-tip polymer microstamp.[60] Figure 5(a) shows a nanowire post-transfer, prior to contact fabrication. Nanowires are aligned parallel to the multiplexer output. Source/drain electrodes are defined by e-beam lithography and metallized with ≃70 nm sputtered Ni after transfer, Figure 5(b). Full details

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Table 2. Contact Resistance, Carrier Density, Mobility, Sub-threshold Swing, on/off Ratio, Threshold Voltages in the up/down Sweep Directions, and Hysteresis $\Delta V_t = V_t(\text{down}) - V_t(\text{up})$, Extracted from Data in Figure 5(e)[a]

channel	R_C (kΩ)	n ($\times 10^{17}$ cm^{-3})	μ_{FE} (cm^2 V^{-1}s^{-1})	SS (mV dec^{-1})	on/off (dec)	V_t(up) (V)	V_t(down) (V)	ΔV_t (V)
9	0.79	39.4	1630−4490	470	3.3	−7.24	−7.01	0.23
10	2.07	38.3	860−2000	140	3.1	−7.1	−6.71	0.39
11	0.51	42.2	1340−4400	450	3.3	−7.82	−7.61	0.21
12	2.03	39.9	810−4050	300	3.1	−7.78	−6.71	1.07
13	2.97	44.2	480−3200	500	3	−8.48	−7.78	0.7
14	1.41	43.9	710−2980	320	3.2	−8.63	−7.5	1.13
16	7.36	37.7	340−1140	850	2.7	−7.16	−6.42	0.74
mean	2.45	40.8	880−3180	430	3.1	−7.74	−7.11	0.64
std	2.32	2.6	460−1260	220	0.2	0.62	0.53	0.38

[a]The mean length of nanowires 9−12 (13−16) is L = 606 (401) nm. Lower and upper bounds for μ_{FE} are given by considering data before and after subtracting for series and contact resistance, respectively.

on the nanowire transfer printing technique can be found in Methods and in refs 60−63.

On channels 1−8 the source and drain contacts are shorted with Ni, and their resistance is used to estimate the series resistance of the multiplexer and circuit. The mean series resistance is R_S = 3.77 kΩ and includes the ohmic/Ni interface and Ni contacts themselves. The mean length of channels 9−12 (13−16) is L = 606 (401) nm. These sets of four are defined to be the same length, set by the separation between source−drain contacts. The average diameter is $W \approx 65$ nm for all nanowires. For channels 10 and 16 single nanowires are transferred. Pairs of nanowires in parallel are transferred to channels 9, 11, 12, 13, and 14. The nanowire at channel 15 became detached during subsequent fabrication. Figure 5(c) shows SEM images of single and pairs of nanowires. In the future, prescreening nanowires using a multistage transfer-printing process[64] or SEM/atomic force microscopy techniques will enable selection of purely single nanowires.

Figure 5(e) shows G as a function of back gate voltage V_G for L = 401 and 606 nm nanowires, in the left- and right-hand columns, respectively. Measurements are performed at T = 4.2 K with the device immersed in liquid helium. The two-terminal differential conductance is measured using a constant source−drain voltage V_{sd} = 10 μV rms at 77 Hz. At high V_G the conductance curve flattens as the total resistance $R = R_{NW} + 2R_C + R_S$ becomes dominated by the series resistance R_S and contact resistance R_C between the nanowires and metal electrodes. Although the nanowire resistance is not negligible,[65−67] this gives an upper limit of R_C from ∼0.5 to 7.4 kΩ across the array.

We estimate the electron density n from the total charge $e(\pi r^2 L)n = C_{NW}\Delta V$, where ΔV is the change in voltage from saturation to threshold using the average threshold voltage V_t for gate sweeps in the up and down directions, and C_{NW} is the gate capacitance from a cylinder-on-plane model[68,69]

$$C_{NW} = \frac{2\pi\epsilon L}{\ln\left(\frac{d + r + \sqrt{(d+r)^2 - r^2}}{r}\right)} \quad (3)$$

For oxide thickness d = 50 nm and nanowire radius r = 32.5 nm, C_{NW} = 0.16 and 0.10 fF for channels 9−12 and 13−16, respectively. The mean density is $n = 40.8 \times 10^{17}$ cm^{-3}, corresponding to an electron−electron spacing of ∼6 nm. We neglect capacitance from surface/interface states.[70]

The field-effect mobility of a nanowire on a planar substrate is given by $\mu_{FE} = g_m L^2/C_{NW}V_{sd}$, where $g_m = \partial I_{sd}/\partial V_G$ is the transconductance, $I_{sd} = GV_{sd}$ is the source−drain current, and V_{sd} is the rms source−drain voltage. This gives μ_{FE} from 1140 to 4490 cm^2 V^{-1} s^{-1} after subtracting for R_S and R_C, with a mean of 3180 cm^2 V^{-1} s^{-1}. This is an upper bound, since R_C is overestimated. Simply taking the raw data without subtracting for either R_C or R_S provides lower bounds of μ_{FE} from 340 to 1630 cm^2 V^{-1} s^{-1}, with a mean of 880 cm^2 V^{-1} s^{-1}.

Two further parameters for quantifying nanowire behavior are the subthreshold swing ($SS = (\partial(\log_{10} I_{sd})/\partial V_G)^{-1}$) and the on/off ratio, taken here as the number of orders of magnitude by which I_{sd} changes between threshold and saturation. Resistance subtraction makes little difference on a log scale near threshold; therefore very similar values for SS are found when resistance is/is not subtracted. The higher number of SS is given as a conservative estimate of device behavior. Table 2 summarizes the calculated parameters for the seven multiplexed nanowires. While data points are too few for statistical comparison, it is a useful demonstration that nanowires can be successfully integrated with the multiplexer without any reduction in quality, since parameters compare favorably to nonmultiplexed WZ nanowires,[69] which showed V_t = −7.4 V, on/off ratio = 3.4 dec, SS = 2320 mV dec^{-1}, $n = 4.7 \times 10^{17}$ cm^{-3}, and μ_{FE} = 340 cm^2 V s^{-1}. These measurements were performed at room temperature, which accounts for the lower mobility and higher SS[71] compared to our devices. The carrier density is larger in our measurements since an ammonium sulfide etch is performed prior to contact deposition to remove native oxide. Although a patterned resist is used to selectively etch only in the contact region, there can be unintentional etching away from the contact region underneath the resist, up to a couple of hundred nm into the nanowire channel. For nanowires with contacts separated by >1 μm a greater proportion of the channel is unaffected (nanowires in ref 69 are several microns long). However, in short channels (<500 nm), it appears that most of the nanowire can be exposed to ammonium sulfide, which can increase surface accumulation, leading to higher carrier densities.[72]

Previously, nanowires are studied either individually or in parallel arrays.[19,20] Multiplexing allows both in a single array. This enables a range of studies, for example the comparison of techniques used to suppress conductance fluctuations in magnetotransport measurements, which can be studied either using gate voltage averaging techniques in individual nanowires[16−18] or by measuring nanowires in parallel.[19,20]

Exfoliated Graphene. An array of mechanically exfoliated graphene flakes is assembled by using a polymer-based dry transfer technique,[35,73] as described in Methods. This is presented as a proof of concept of compatibility with exfoliated 2D materials and van der Waals heterostructures (multilayer 2D material stacks),[74] which are created using this transfer

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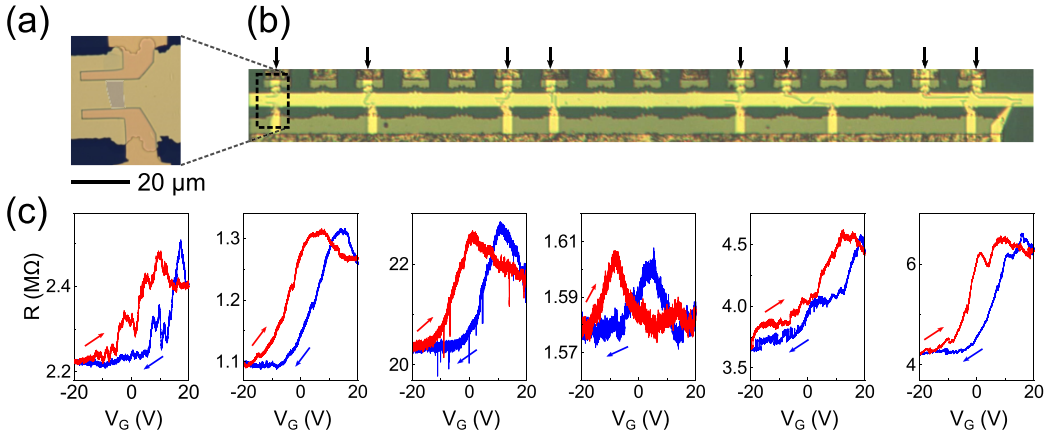

Figure 6. Multiplexed arrays of exfoliated graphene. (a) Exfoliated graphene device connected to channel 1. Source−drain electrodes connect to the multiplexer output and common drain. The device active area is highlighted in blue (false color), for clarity. (b) Graphene flakes are connected to eight multiplexer channels, indicated by the arrows. (c) Resistance as a function of back gate voltage (V_G) for channels 6, 7, 11, 12, 15, and 16 (left-to-right); devices on channels 1 and 3 do not conduct. Arrows indicate the gate voltage sweep direction.

technique and used to research a wide variety of quantum phenomena.

Eight monolayer graphene flakes are transferred to the multiplexer. A close-up of one device is shown in Figure 6(a), with graphene highlighted in blue (false color). Source−drain contacts (≈100 nm Cr/Au) connecting the graphene to multiplexer output channels and the common drain are fabricated after transfer. Figure 6(b) shows the device array; arrows indicate channels with graphene attached. A 75% yield is achieved since channels 1 and 3 show open-circuit behavior. The proximity of flakes is set by the size of the polymer stamp, here ∼2 × 2 mm. Larger arrays can be created by reducing the stamp size, using a flat-tip microstamp[60] or a stamp formed by a drop of Elvacite/anisole solution.[75] Alternatively, the distance between multiplexer outputs may be increased.

Figure 6(c) shows the resistance as a function of V_G for six devices. Red (blue) show gate voltage sweeps in the up (down) direction, for measurements at $T = 4.2$ K. DC measurements are performed with a large DC bias $V_{dc} = -500$ mV since IV curves showed nonlinear behavior as V_{dc} is swept, similar to when a Schottky barrier exists between the graphene and contacts.[76,77] We estimate contact resistivity $\rho_C = 1.27, 0.31, 3.51, 0.06, 1.37, 1.79 \times 10^7$ Ω μm for devices on channels 6, 7, 11, 12, 15, and 16, respectively, using $\rho_C = R_C W$, with $W = 12, 7.5, 3.7, 0.7, 7.8$, and 12.2 μm and $R_C = 1.06, 0.42, 9.47, 0.79, 1.76$, and 1.47 MΩ. Equation 1 is used to find R_P, and we approximate $R_C = R_P/2$, since the contact resistance dominates over all other series resistance terms. Previously, resistivities between 10^3 and 10^6 Ω μm have been reported for Cr/Au contacts on graphene without specifically mentioned contact optimization,[78] and reasonable variability is not unexpected.[79] The high resistivity of our devices and nonlinearity of dc bias suggest the existence of an unintentional interlayer between the metal and the graphene, such as polymer residues, and likely arises from contamination during the transfer procedure. Our graphene flakes are picked up directly by the polymer stamp and transferred to the multiplexer, in contrast to typical dry transfer, where a hBN encapsulation layer is picked up prior to the graphene to create a stack[35,73] and prevents the graphene from being exposed to transfer materials and chemicals, resulting in much higher device performance and clean contact interfaces. For comparison ρ_C for our CVD pristine devices varies from ∼1 to 2×10^5 Ω μm, with the same assumption that $R_C = R_P/2$.

Lower contact resistances are achievable, and a comprehensive list of contact resistivities for different metals/processes for CVD and exfoliated graphene is available in ref 80. Resistivities as low as 23 Ω μm have been reported[81,82] by optimizing contact metals and methodologies. There is no intrinsic reason why low resistance cannot be achieved with the multiplexer by improving the contact fabrication and transfer, using techniques such as edge contacts to 2D materials encapsulated in hexagonal boron nitride,[35] cleaning of contact areas with an oxygen plasma[36,37] or UV ozone[38] prior to metallization, thermal annealing,[37,39,40] different contact metals,[80] patterning holes or cuts in the graphene underneath the contacts,[34,82] fabrication in a glovebox environment,[75,83] n-doping graphene combined with edge contacts,[81] or shadow mask evaporation.[84] Since our emphasis is on high-throughput testing, techniques that can be globally applied during fabrication give the most scalable solution. This would include options such as glovebox fabrication in which graphene is not exposed to ambient conditions, shadow mask evaporation, which avoids use of resists, or plasma/ozone cleaning.

In Figure 6(c) the Dirac point occurs at positive V_G for most devices, reflecting unintentional p doping from moisture and oxygen adsorption after exposure to ambient conditions. The hysteresis in gate voltage sweeps, $\Delta V_{CNP} = V_{CNP}(\text{down}) - V_{CNP}(\text{up})$, is used to estimate a carrier trap density at the graphene−Al_2O_3 interface from the corresponding change in carrier density $\Delta n = C_G \Delta V_{CNP}/e$,[46] giving $\Delta n = 3, 3.5, 4.2, 5.9, 2.6$, and 3.2×10^{12} cm^{-2} for channels 6, 7, 11, 12, 15, and 16, respectively. The large hysteresis reflects the quality of the graphene−Al_2O_3 interface, post-transfer processing, and exposure to ambient conditions, which was not mitigated against for these devices.

With improvement the multiplexer will become a useful tool for testing arrays of many types of exfoliated 2D materials and van der Waals heterostructures, which are created using the same pick-up-and-place transfer system as used here.[35,73] Different material configurations and geometries can be tested side-by-side. Automated assembly[75] may also allow rapid creation of large arrays. More exotic devices can also be combined with the multiplexer, for example arrays of single electron/single molecular transistors using nanoparticles in nanogaps.[5,6] The potential for the multiplexing geometry is significant in the fabrication of quantum circuits, where adding a

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multiplexer creates built-in redundancy by selecting one device from an array. This is particularly important for devices with low yield, such as those with quantum effects that are only realized in critical geometric combinations. As initial next innovations to reduce standard deviation and increase yield for all types of arrays studied here we suggest investigating encapsulation[44−47] and thermal annealing[37,39,40] to achieve higher mobilities and lower contact resistances and to reduce exposure to environmental conditions. Edge contact methods should also be investigated for the 2D materials.[34,35]

The multiplexer can be used from room temperature to cryogenic temperatures, which allows the study of temperature-dependent behavior of transistors and quantum devices. In this case the temperature-dependence of the 2DEG resistance is also relevant.[85] For many devices, such as those presented in this paper, the series resistance can be extracted at each temperature by analyzing transfer characteristics. Two further options are possible with future design innovations, either to measure the 2DEG resistance directly or circumvent the series resistance altogether using four probe measurements. First, there is much benefit to fabricating future multiplexers with one channel shorted to the common drain and using this channel to measure the 2DEG resistance directly. This term can then be used in analysis of multiplexed devices on that chip. A second, important innovation is to achieve four probe measurements of multiplexed devices, for example by adding an insulating layer on top of the multiplexer to allow metal gates to be routed into the nanodevice area, which can be connected to individual devices.

CONCLUSIONS

A single multiplexer design is presented to measure individual devices within arrays of nanomaterials. Three different arrays are measured—CVD-grown graphene, InAs nanowires, and mechanically exfoliated graphene flakes—with devices transferred by wet and dry processes. The multiplexer can be operated at room temperature to check devices are connected prior to cooling to milli-Kelvin temperatures. Key parameters are extracted to quantify electronic performance including mobility, residual carrier density, and parasitic/contact resistance for CVD graphene devices and density, mobility, subthreshold swing, and on/off ratio for nanowires. Values similar to nonmultiplexed devices are found, showing integration with the multiplexer is not detrimental to performance. Mechanically exfoliated monolayer graphene flakes transferred using a polymer-based dry transfer technique are measured as a proof of concept that 2D material flakes and van der Waals heterostructure devices can also be multiplexed. Low-resistance contact fabrication techniques are required for future arrays; data are presented here without optimized contact fabrication as a proof of concept.

The multiplexer technique applied to 2D materials, to nanowires, and potentially to colloidal particles in nanogaps and molecules in graphene nanogaps is a shift from individual testing of devices and multiple repetitions of fabrication/measurement to a scalable and efficient approach that measures many devices in a single experimental run. The multiplexer is universally compatible to many kinds of nanoelectronic devices beyond those presented here. Large data sets can be gathered for ensemble assessment, as well as speeding up the search for individual devices with exotic phenomena occurring when precise/opportunistic fabrication conditions are met.

METHODS

GaAs Multiplexer. The multiplexer conduction path is defined in a GaAs high electron mobility transistor, and the mesa is defined by chemical etching. Multiplexers for CVD and exfoliated graphene are fabricated on Cavendish wafer V832, and the nanowire multiplexer is fabricated on Cavendish wafer V684. The 2DEG forms 90/70 nm below the surface for wafers V832/V684. For V832, the mean sheet density and electron mobility are $n = 1.53 \times 10^{11}$ cm^{-2} and $\mu = 8.17 \times 10^5$ cm^2 V^{-1} s^{-1}, respectively, measured on a separate Hall bar device. For V684, Hall bar measurements gave $n = 2.49 \times 10^{11}$ cm^{-2} and $\mu = 4.20 \times 10^5$ cm^2 V^{-1} s^{-1}. Ohmic contacts are created at the source and 16 outputs, and a 10/40 nm thick Ti/Au back gate is defined adjacent to the outputs. An Al_2O_3 gate dielectric is deposited by ALD, and the dielectric thickness is 110, 94, and 50 nm for multiplexers of CVD-grown graphene, exfoliated graphene, and nanowires, respectively. Windows are etched over bond pads, ohmic contacts, and multiplexer channels as necessary, *e.g.*, above channel L in Figure 1(c). A second Al_2O_3 layer of 15 nm thick is deposited on the CVD graphene multiplexer, and windows are etched above bond pads and ohmic contacts, which allows this multiplexer to be tested at room temperature. Addressing gates (Ti/Au) are deposited at a slight rota-tilt angle (10−15°) to facilitate continuity over the etched mesa edge.

The total parasitic resistance in the circuit is $R_P = 2R_C + R_{2DEG} + R_{ohmic} + R_{wiring}$, where resistances of the multiplexer 2DEG, ohmic contacts, circuit/cryostat wiring, and contact electrodes to the device under test are denoted by R_{2DEG}, R_{ohmic}, R_{wiring}, and R_C, respectively. A multiplexer with outputs wire bonded to the common drain is measured in a He-3 cryostat with a base temperature of $T = 0.28$ K. The mean resistance of 15 channels is $R = 469\ \Omega$ (one channel was not connected). Assuming negligible resistance from the wire bonds (*i.e.*, $R_C = 0$), this is an estimate of the upper limit of resistances $R_{2DEG} + R_{ohmic} + R_{wiring}$. The largest component is likely to be R_{2DEG}, since the expected channel-dependent 2DEG resistance through the multiplexer is $R_{2DEG} \lesssim 500\ \Omega$, estimated using carrier density $n = 1.53 \times 10^{11}$ cm^{-2} for this wafer (V832).

Wet Transfer of CVD Graphene. Monolayer graphene films are grown by chemical vapor deposition on Cu. The graphene/Cu substrate is coated on one side by PMMA, and graphene is removed from the unprotected side by reactive-ion etching (RIE) with an oxygen plasma. The PMMA−graphene−Cu stack is floated on the surface of a 1.2% solution of ammonium persulfate etchant $(NH_4)_2S_2O_8$, with the Cu side in contact with the $(NH_4)_2S_2O_8$. A 1 × 1 cm^2 stack is etched for approximately 6 h to ensure the Cu is dissolved. The PMMA−graphene is rinsed by transferring to the surface of a DI water bath for 1 min and to a second DI water bath for 1 h. The PMMA−graphene stack is lifted from the DI water using the target substrate and dipped in isopropyl alcohol (IPA) for a few seconds, before drying in air overnight. The sample is baked at 125 °C prior to removing the PMMA to improve adhesion of graphene to the target substrate. For this study CVD graphene devices are defined by photolithography and are contacted from below by electrodes fabricated prior to transfer. Graphene is removed from the rest of the chip using an oxygen reactive ion etch, 30 W power for 1 min.

Exfoliated Graphene Arrays. Graphene is exfoliated onto a SiO_2 substrate cleaned by reactive ion etching in an O_2 plasma. Monolayer flakes are picked up and transferred to the multiplexer using a polymer stack of polydimethylsiloxane (PDMS) block/polycarbonate (PC) film on a glass slide. Flakes are transferred one at a time. After four flakes are transferred the multiplexer chip is immersed in chloroform to dissolve the PC film and then rinsed in IPA. Four more flakes are transferred followed by a second immersion in chloroform and IPA. Contacts are defined by e-beam lithography; ∼100 nm total thickness Cr/Au is deposited using electron beam evaporation.

Nanowire Transfer. Given the ultrasmall dimensions of the InAs nanowires (diameter ∼65 nm, length ∼600 nm), the transfer-printing process for their integration onto the multiplexer is done in three stages: (1) InAs NWs are captured in bulk from their growth substrate using a large, ∼1 mm^2, PDMS block and applying shear motion against the NW direction on the growth substrate. The captured NWs are subsequently

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transferred in bulk onto an intermediate PDMS surface. (2) The bulk-transferred InAs NWs are then visually assessed, and selected NW devices arranged in 1D arrays against a reference point in the intermediate PDMS sample. The 1D arrays of InAs NWs are mapped using a high-resolution optical microscope to ensure they are undamaged and in suitable condition for final integration in the multiplexer. (3) The final selected InAs NWs are captured from their location in the formed 1D NW arrays by means of a polymeric (PDMS) μ-stamp (surface area 10×30 μm) and precisely transfer-printed onto the target locations on the multiplexer back gate with controlled orientation.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acsnano.0c05622.

Scanning electron microscope images of CVD graphene devices and mean free path calculations (PDF)

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Notes

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