

# Dirac-Point Shift by Carrier Injection Barrier in Graphene Field-Effect Transistor Operation at Room Temperature

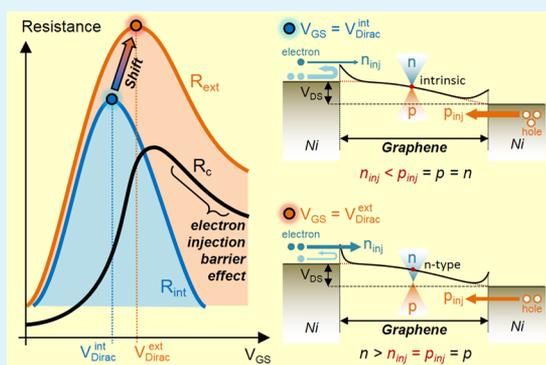
Sungsik Lee,<sup>†</sup> Arokia Nathan,<sup>\*</sup> Jack Alexander-Webber,<sup>‡</sup> Philipp Braeuninger-Weimer,<sup>‡</sup> Abhay A. Sagade,<sup>‡</sup> Haichang Lu, David Hasko, John Robertson, and Stephan Hofmann<sup>‡</sup>

Electrical Engineering Division, Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge, CB3 0FA, United Kingdom

## Supporting Information

**ABSTRACT:** A positive shift in the Dirac point in graphene field-effect transistors was observed with Hall-effect measurements coupled with Kelvin-probe measurements at room temperature. This shift can be explained by the asymmetrical behavior of the contact resistance by virtue of the electron injection barrier at the source contact. As an outcome, an intrinsic resistance is given to allow a retrieval of an intrinsic carrier mobility found to be decreased with increasing gate bias, suggesting the dominance of short-range scattering in a single-layer graphene field-effect transistor. These results analytically correlate the field-effect parameters with intrinsic graphene properties.

**KEYWORDS:** graphene field effect transistor, Dirac point, Fermi velocity, asymmetric injection, intrinsic carrier mobility, short-range scattering



Ever since graphene was identified as a promising electronic material for newly emerging applications, there have been numerous studies on its material properties and associated device performance.<sup>1–8</sup> This has led to a study of new device architectures and, in particular, attempts to identify the role of contact materials with the graphene layer,<sup>9–11</sup> suggesting that contact properties significantly limit the performance of graphene devices. At the same time, there has been equally important emphasis on the study of the intrinsic electronic properties of “bulk” graphene.<sup>4–6</sup> For example, it has been reported that the Dirac cones of a suspended graphene layer are reshaped by carrier interaction effects associated with the carrier density in graphene.<sup>8,12</sup> However, when used as the channel in a field-effect device, it is important to understand how the graphene material properties correlate with device characteristics. In this regard, it has been reported that the Dirac point can be shifted due to contact properties at the source and drain electrodes, which was observed either by a four-point probe measurement at low temperatures,<sup>13</sup> (e.g., 60 K), or by employing different work-function metals for the source and drain electrodes.<sup>14–16</sup> Although there have been previous studies on the effects of contacts on graphene field-effect devices, these have not been used to understand how the intrinsic properties, such as contact effects, Dirac point, carrier density, and intrinsic carrier mobility, are influenced at room temperature by an orthogonal electric field, and their interrelation in a field-effect structure. This constitutes the focus of the investigations presented in this work.

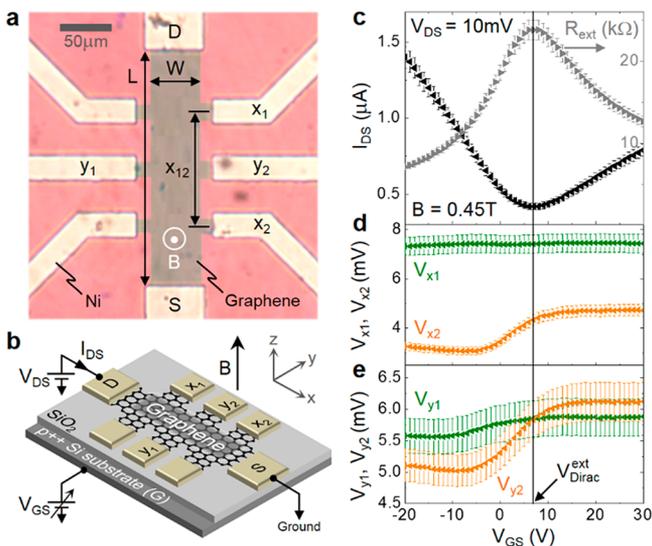
Using a combination of Hall-effect and Kelvin-probe measurements at room temperature, we examine the symmetry in the behavior of the intrinsic resistance, as a function of gate bias, retrieved from the incongruity in the contact and extrinsic resistances of the device. The resulting positive shift in the extrinsic Dirac point, from that of the intrinsic counterpart is explained by the asymmetrical behavior of the contact resistance as a function of gate bias, suggesting the presence of an injection barrier for electrons by virtue of the higher work-function of the nickel (source contact) electrode, compared to the graphene layer. In addition, Dirac voltage is observed to be the common intercept for the linear variation in electron and hole carrier densities. From the extracted intrinsic resistance and carrier density, the intrinsic carrier mobility is retrieved showing its decrease with increasing gate bias. This suggests dominance of short-range scattering, the rate of which can increase as more carriers are induced by a higher gate bias, and has been observed previously in single-layer graphene. These results provide analytical insight into the underlying physics across the field-dependent intrinsic parameters, while maintaining a consistency with earlier reports.

Figure 1 shows representative results from Hall-effect measurements coupled with Kelvin-probe measurements of a graphene field-effect transistor; the detailed fabrication process

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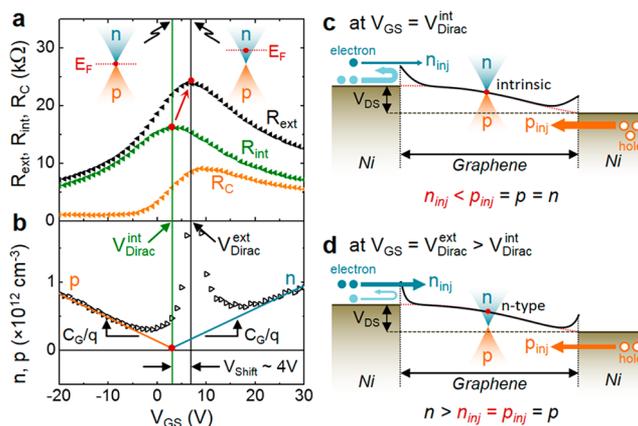


**Figure 1.** Hall-effect and Kelvin-probe measurements on the graphene field-effect transistor: (a) Microphoto of the fabricated structure and its (b) 3-D view along with the electrical measurement setup. Here, the channel length ( $L$ ), width ( $W$ ), and vertical separation ( $x_{12}$ ) are  $250 \mu\text{m}$ ,  $50 \mu\text{m}$ , and  $120 \mu\text{m}$ , respectively. (c) Measured drain current ( $I_{\text{DS}}$ ) at  $V_{\text{DS}} = 10 \text{ mV}$  and the equivalent resistance ( $R_{\text{ext}} = V_{\text{DS}}/I_{\text{DS}}$ ), as a function of  $V_{\text{GS}}$  for  $B = 0.45 \text{ T}$ . (d) Measured  $V_{x1}$  and  $V_{x2}$ , as a function of  $V_{\text{GS}}$ , and (e) measured  $V_{y1}$  and  $V_{y2}$  as a function of  $V_{\text{GS}}$ . Here, the measured data in panels (c)–(e) have error bars of 5%.

has been published elsewhere<sup>17,18</sup> and can also be found in the Supporting Information. The photomicrograph of the measured test structure is shown in Figure 1a. The electrodes on the  $x$ -axis are used to measure the internal voltage drops and those on the  $y$ -axis are used to measure the Hall voltage ( $V_{\text{H}}$ ). The source (S) and drain (D) electrodes are on an oxidized high-doped silicon wafer, which serves as the gate (G). The gate bias ( $V_{\text{GS}}$ ) is swept at a constant drain bias ( $V_{\text{DS}}$ ) in the presence of a magnetic field ( $B$ ) applied orthogonally (i.e., along the  $z$ -axis) and uniformly over the graphene layer. Along with this, a drain current ( $I_{\text{DS}}$ ) at a small drain bias ( $V_{\text{DS}}$ ) and the equivalent extrinsic resistance (i.e.,  $R_{\text{ext}} = V_{\text{DS}}/I_{\text{DS}}$ ) are measured as a function of  $V_{\text{GS}}$  for  $B = 0.45 \text{ T}$ , as seen in Figure 1c. Here,  $V_{\text{DS}}$  is fixed at  $10 \text{ mV}$ , which is sufficiently smaller than the gate bias and thermal voltage ( $\sim 26 \text{ mV}$  at room temperature, i.e.,  $300 \text{ K}$ ) to satisfy the gradual channel approximation.<sup>19</sup> In addition, the voltage levels ( $V_{x1}$ ,  $V_{x2}$ ) at the nodes of  $x_1$  and  $x_2$  are measured while measuring the voltage levels ( $V_{y1}$ ,  $V_{y2}$ ) at the nodes  $y_1$  and  $y_2$ , as a function of  $V_{\text{GS}}$ , respectively (see Figures 1d and 1e, respectively). Here, the extrinsic Dirac voltage (i.e.,  $V_{\text{Dirac}}^{\text{ext}}$ ) is retrieved at the minimum point of  $I_{\text{DS}}$  (i.e., the peak of  $R_{\text{ext}}$ ), which is consistent with  $V_{\text{GS}}$  at which  $V_{y1} = V_{y2}$ . Note that the extrinsic Dirac voltage can be shifted due to atmospheric absorption.<sup>19</sup>

Based on the experimental results discussed with Figure 1, the gate-voltage dependence of the intrinsic parameters of the graphene device is shown in Figure 2. First, the contact resistance ( $R_{\text{C}}$ ) is found from the difference between  $R_{\text{ext}}$  and the intrinsic resistance ( $R_{\text{int}}$ ), i.e.,  $R_{\text{C}} = R_{\text{ext}} - R_{\text{int}}$ , which are functions of  $V_{\text{GS}}$ , respectively. Here,  $R_{\text{int}}$  is described by the following relation:

$$R_{\text{int}} = \left( \frac{V_{x1} - V_{x2}}{I_{\text{DS}}} \right) \frac{L}{x_{12}} \quad (1)$$



**Figure 2.** Gate-voltage dependence of intrinsic parameters of the graphene transistor and underlying band diagram illustrating electron and hole injection: (a) Retrieved  $R_{\text{C}}$  from the difference between  $R_{\text{ext}}$  and  $R_{\text{int}}$ . (b) Extracted concentrations of the free electrons ( $n$ ) and holes ( $p$ ), as a function of  $V_{\text{GS}}$ . (c) Conceptual band diagram to describe the blocking of electron injection at  $V_{\text{GS}} = V_{\text{Dirac}}^{\text{int}}$ . (d) Conceptual band diagram at  $V_{\text{GS}} = V_{\text{Dirac}}^{\text{ext}}$ .

where  $x_{12}$  is the distance between the electrodes  $x_1$  and  $x_2$ , as indicated in Figure 1a. It is observed that the peak point of  $R_{\text{ext}}$  (i.e., extrinsic Dirac voltage,  $V_{\text{Dirac}}^{\text{ext}}$ ) is right-shifted by  $4 \text{ V}$  from that of  $R_{\text{int}}$  (i.e., intrinsic Dirac voltage,  $V_{\text{Dirac}}^{\text{int}}$ ) (see Figures 2a and 2b). This suggests the presence of an electron injection barrier, corresponding to the asymmetrical characteristics of  $R_{\text{C}}$ , as a function of  $V_{\text{GS}}$ , as can be seen in Figure 2a. Note that, if there was a hole injection barrier, this would be shifted the opposite way. Here, the sign of  $V_{\text{Dirac}}^{\text{int}}$  is positive, as seen in Figure 2a, suggesting that the graphene layer is  $p$ -type as its initial polarity. Note that  $V_{\text{Dirac}}^{\text{ext}}$  is widely used as a signature of the polarity of the graphene layer. However, it can be wrong, depending on the extent of the shift voltage, i.e.,  $V_{\text{Shift}} \equiv V_{\text{Dirac}}^{\text{ext}} - V_{\text{Dirac}}^{\text{int}}$ . For example, if  $V_{\text{Shift}} > V_{\text{Dirac}}^{\text{int}}$  (i.e.,  $V_{\text{Dirac}}^{\text{int}} < 0$ ), the graphene layer would be  $n$ -type.

To explain this theoretically, a conceptual band diagram is shown in Figures 2c and 2d. First, Figure 2c shows the impeded electron injection at  $V_{\text{GS}} = V_{\text{Dirac}}^{\text{int}}$ , before  $R_{\text{ext}}$  reaches its peak, in which the injected electron density ( $n_{\text{inj}}$ ) is still less than the injected hole density ( $p_{\text{inj}}$ ), even when  $n = p = p_{\text{inj}}$  in the graphene layer at  $V_{\text{GS}} = V_{\text{Dirac}}^{\text{int}}$ . Here,  $n$  and  $p$  are the respective free electron and hole densities within the graphene layer. In contrast,  $R_{\text{ext}}$  at  $V_{\text{GS}} = V_{\text{Dirac}}^{\text{ext}}$  now exhibits its peak when there is sufficient electron injection due to higher gate bias, resulting in  $n_{\text{inj}} = p_{\text{inj}} = p < n$ , as indicated in the conceptual band diagram seen in Figure 2d. Here, a higher gate bias induces more electrons in the channel, making the Schottky barrier narrower at the source contact, eluding to higher electron injection ( $n_{\text{inj}}$ ). When  $n_{\text{inj}}$  is balanced with injected holes ( $p_{\text{inj}}$ ), the extrinsic resistance ( $R_{\text{ext}}$ ) exhibits its peak at  $V_{\text{GS}} = V_{\text{Dirac}}^{\text{ext}}$ .

We now extract the free electron ( $n$ ) and hole ( $p$ ) densities within the graphene layer from the Hall-effect measurements (see Figure 1e), each as a function of  $V_{\text{GS}}$ , using the following relation:<sup>20–22</sup>

$$n, p = \left| \frac{I_{\text{DS}} B}{q(V_{y1} - V_{y2})} \right| \quad (2)$$

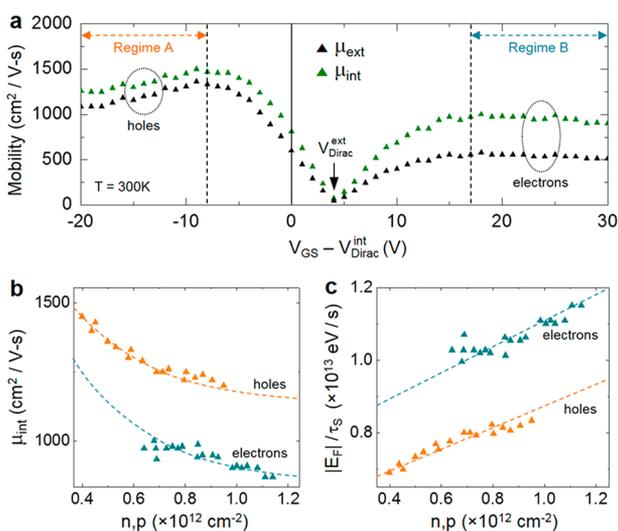
where  $q$  is the elementary charge. As seen in Figure 2b, the extrapolation lines for electrons and holes converge at  $V_{\text{Dirac}}^{\text{int}}$

rather than at  $V_{\text{Dirac}}^{\text{ext}}$ . This further confirms that the peak of  $R_{\text{int}}$  is the intrinsic point for  $n = p$ . Here, the slope of the extrapolation line is proportional to the gate capacitance ( $C_G$ ), as labeled in Figure 2b.

Using the results in Figures 2a and 2b, a field-effect mobility of the graphene transistor can be retrieved. In addition, there are two types of the field-effect mobility, depending on whether the contact effect resides. One of them is the intrinsic carrier mobility ( $\mu_{\text{int}}$ ), where the contact effect is removed. Moreover, it can be extracted using the following macroscopic definition:<sup>19</sup>

$$\mu_{\text{int}} = \frac{1}{R_{\text{int}} Q_{n,p}} \quad (3)$$

where  $Q_{n,p} = C_G |V_{\text{GS}} - V_{\text{Dirac}}^{\text{int}}| = qn$  or  $qp$ . Similarly, the extrinsic mobility ( $\mu_{\text{ext}}$ ) with the contact effect, as the other type, can be defined as  $\mu_{\text{ext}} = (R_{\text{ext}} Q_{n,p})^{-1}$ . Figure 3a shows the extracted  $\mu_{\text{int}}$



**Figure 3.** Field-effect mobility and carrier density. (a) Mobility ( $\mu_{\text{int}}$  and  $\mu_{\text{ext}}$ ), as a function of  $V_{\text{GS}}$  calibrated with  $V_{\text{Dirac}}^{\text{int}}$ . Here, regimes A and B show the mobility decays. (b) Intrinsic mobility ( $\mu_{\text{int}}$ ) vs the carrier density ( $n, p$ ). (c) Fermi energy per scattering time ( $|E_F|/\tau_s$ ), as a function of the carrier density ( $n, p$ ). Here, the dotted lines denote the fitted trends.

and  $\mu_{\text{ext}}$  for electrons and holes, respectively. As can be seen,  $\mu_{\text{int}}$  is higher than  $\mu_{\text{ext}}$ . In particular, the difference between  $\mu_{\text{int}}$  and  $\mu_{\text{ext}}$  for electrons is much higher than the case of the hole mobility. This reflects the asymmetrical behavior of the contact resistance, as a function of gate bias, as discussed earlier with Figure 2a. As another observation from Figure 3a, the  $\mu_{\text{int}}$  for both electrons and holes is found to be decreased as the gate bias increased. Since the carrier density is linearly proportional to the gate voltage in regimes A and B, i.e.,  $qn, qp = C_G |V_{\text{GS}} - V_{\text{Dirac}}^{\text{int}}|$ , where each carrier mobility decays (see also Figure 2b),  $\mu_{\text{int}}$  can be replotted as a function of the carrier density, as shown in Figure 3b. From this, we find that  $\mu_{\text{int}}$  is inversely proportional to the carrier density. This behavior can be explained with the short-range scattering model.<sup>23–25</sup> This trend is consistent with the expected behavior of a single-layer graphene transistor.<sup>24,25</sup>

In order to explain the intrinsic mobility behavior, the following microscopic definition of the intrinsic mobility, based on the short-range scattering model, is employed:<sup>24</sup>

$$\mu_{\text{int}} = \frac{qv_F^2 \tau_s}{|E_F|} \quad (4)$$

where  $v_F$  is the Fermi velocity,  $\tau_s$  the short-range scattering time, and  $E_F$  the Fermi energy. From eqs 3 and 4, the carrier density ( $n, p$ ) is represented as a function of  $|E_F|/\tau_s$ ,

$$n, p = \left( \frac{1}{q^2 v_F^2 R_{\text{int}}} \right) \frac{|E_F|}{\tau_s} \quad (5)$$

With eq 5, the correspondence between the carrier density and  $|E_F|/\tau_s$  is computed for  $v_F = 10^8$  cm/s, as seen in Figure 3c, clearly confirming their proportionality.<sup>24,25</sup> These results indicate that the dominance of the short-range scattering is proportional to the carrier density in a single-layer graphene-based field-effect transistor.

A combination of Hall-effect measurements and Kelvin-probe measurements shows a shift in the extrinsic Dirac point from the intrinsic counterpart, suggesting the presence of an electron injection barrier and, hence, asymmetrical contact resistance, as a function of gate bias. This indicates that the Dirac point is shifted by not only the polarity of the graphene layer but also by the contact properties at the source and drain junctions. In addition, the intrinsic carrier mobility is found to be decreased as the gate bias increased, which is due to an increased short-range scattering of induced carriers in a single layer graphene-based field effect transistor. These results provide analytical physical insight into the correlation between the field-effect parameters and intrinsic material properties.

## ■ ASSOCIATED CONTENT

### Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsami.8b02294.

Discussion of graphene growth and device fabrication, as well as device encapsulation; Figures S1 and S2 (PDF)

## ■ AUTHOR INFORMATION

### Corresponding Author

\*E-mail: an299@cam.ac.uk.

### ORCID

Sungsik Lee: 0000-0002-5523-8476

Jack Alexander-Webber: 0000-0002-9374-7423

Philipp Braeuninger-Weimer: 0000-0001-8677-1647

Stephan Hofmann: 0000-0001-6375-1459

### Present Addresses

<sup>†</sup>Department of Electronics Engineering, Pusan National University, Pusan 46241, Republic of Korea.

<sup>‡</sup>SRM Research Institute and Department of Physics, SRM Institute of Science and Technology, Kattankulathur 603 203, Tamil Nadu, India.

### Author Contributions

S.L. and A.N. designed the experiment and performed analysis. J.A.-W., P.B.-W., A.A.S., and S.H. prepared the samples. D.H. checked the theory and analysis. S.L. and A.N. wrote the manuscript while getting feedback from all other authors.

### Notes

The authors declare no competing financial interest.

All research data are available in the Cambridge University's repository (<https://doi.org/10.17863/CAM.21238>).

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## NOTE ADDED AFTER ASAP PUBLICATION

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