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Atomic layer deposited oxide films as protective interface layers for integrated graphene transfer

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Abstract

The transfer of chemical vapour deposited graphene from its parent growth catalyst has become a bottleneck for many of its emerging applications. The sacrificial polymer layers that are typically deposited onto graphene for mechanical support during transfer are challenging to remove completely and hence leave graphene and subsequent device interfaces contaminated. Here, we report on the use of atomic layer deposited (ALD) oxide films as protective interface and support layers during graphene transfer. The method avoids any direct contact of the graphene with polymers and through the use of thicker ALD layers ($\geqslant$100 nm), polymers can be eliminated from the transfer-process altogether. The ALD film can be kept as a functional device layer, facilitating integrated device manufacturing. We demonstrate back-gated field effect devices based on single-layer graphene transferred with a protective Al_2O_3 film onto SiO_2 that show significantly reduced charge trap and residual carrier densities. We critically discuss the advantages and challenges of processing graphene/ALD bilayer structures.

Supplementary material for this article is available online

Keywords: graphene, transfer, chemical vapour deposition, atomic layer deposition

(Some figures may appear in colour only in the online journal)

Introduction

The development of scalable integrated manufacturing pathways for graphene and related 2D materials is crucial to all their emerging applications and industrial development. Significant progress has been made in 2D crystal growth [1–3], and monolayer graphene crystals beyond the cm-scale [4] and continuous films over areas just limited by the growth reactor geometry [5–7] are now routinely achieved by chemical vapour deposition (CVD). The graphene CVD process utilises a catalytic substrate to achieve high crystallinity [2, 8–10] and for the

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majority of emerging applications the graphene has to be released from this parent growth substrate and transferred into the device stack. To achieve such graphene transfer cleanly and without damage, in order that the unique properties of graphene are preserved, has become a critical challenge [11–15]. This challenge is particularly highlighted by the many proposed (opto-)electronic graphene devices, starting with simple gated graphene field effect device structures, for which the graphene performance is found to be highly sensitive to the presence of any contaminants [16–19]. Most polymer [20–24] and metal [25, 26] layers used as temporary mechanical supports during graphene transfer have been shown to leave residues on graphene after removal, degrading its electronic properties [12, 27, 28]. Other common contaminants include lithographic resists, organic solvents, etching products and ambient air [29], all of which can for instance unintentionally dope the graphene (generally p-type [17]) and cause hysteresis in field effect devices [30]. Hence, ideally the graphene should be protected from any such contamination during transfer and processing as well as during device operation. A number of approaches have been proposed in recent literature to address these challenges. The cleanest graphene device interfaces have been achieved via van-der-Waals heterostructures, particularly graphene sandwiched between h-BN crystals [31–33], using dry transfer techniques which, however, have limited scalability and rely on the availability and quality of other 2D materials. The use of different polymer layers to support graphene transfer and act as part of optoelectronic devices has also been reported but this is limited to certain applications [34–36]. Thin (∼1 nm) metal oxide layers such as Al_2O_3, TiO_2, NiO and Cr_2O_3 directly evaporated onto graphene prior to transfer have been used as protection from direct polymer exposure [37]. Whereas graphene encapsulation with atomic layer deposited (ALD) alumina at the post-transfer stage has enabled reproducible device behaviour with negligible gate hysteresis and low doping levels [38–40]. Due to its scalability and atomic layer growth control, ALD is particularly suited to be used in conjunction with CVD graphene, and initial progress has been made in exploring the ALD parameter space to achieve conformal nucleation of ultrathin oxides on graphene and to improve rational 2D/non-2D material integration [41–44].

Here, we explore the concept of using ALD oxide films for CVD graphene device fabrication in a combined, integrated fashion where the same ALD layer can serve as graphene protection, support, encapsulation and functional device layer. The method avoids any direct contact of the graphene with polymers and through the use of thicker ALD layers (⩾100 nm), polymers can be eliminated from the transfer-process altogether. We focus on alumina (Al_2O_3), hafnia (HfO_2) and titania (TiO_2) ALD layers based on their extensive use in electronic devices as, for instance, high-κ dielectric [38, 42], tunnel barrier [42, 45] or permeation barrier [46, 47]. We demonstrate back-gated field effect devices based on single-layer graphene transferred with a protective Al_2O_3 film onto SiO_2 that show significantly reduced charge trap and residual carrier densities. We critically discuss the advantages and challenges of such integrated approaches, and in particular how this relates to the processing of graphene/ALD bilayer structures.

Methods

Graphene is synthesized by CVD in a commercially available Aixtron BM Pro (4 inch) machine using polycrystalline Cu foils (Alfa Aesar, 25 μm thick, 99.8% purity). Catalysts are annealed for 30 min at 50 mbar in a mixture of H_2/Ar at 1065 °C. CH_4 diluted to 0.1% in Ar is then introduced to the chamber for 45 min promoting growth under a CH_4/H_2/Ar atmosphere and finally cooled down to room temperature in Ar [48].

A Cambridge Nanotech Savannah System (S100 G1) was employed for the deposition of the oxide layers. H_2O was used as oxidant during ALD and the precursors for titania, alumina and hafnia were tetrakis(dimethylamido)titanium (TDMAT, purity >99% Sigma Aldrich 669008), trimethylaluminum (TMA, purity >98%, Strem Chemicals 93-1360) and tetrakis (dimethylamido)hafnium (TDMAHf, purity >99% Sigma Aldrich 455199) respectively. Precursors are volatised at temperatures of 40 °C for H_2O and TMA and 75 °C for TDMAT and TDMAHf. All samples are loaded and unloaded while the chamber is at deposition temperature (200 °C for hafnia and alumina and 120 °C for titania). Before the ALD deposition, the chamber is pumped to reach a base pressure of $\sim 6 \times 10^{-1}$ mbar and purged with 20 sccm N_2 for 10 min. Oxidant and precursors are alternately introduced into the chamber in a 20 sccm flow of N_2 carrier gas, which is the same flow employed during the purging time. Recipes were optimised to provide a continuous film. Details of the ALD growth can be found in the supporting information, available online at stacks.iop.org/NANO/28/485201/mmedia.

Polymer-supported graphene transfer is performed by depositing poly methyl methacrylate (PMMA) onto the graphene/metal-catalyst sample. The catalyst is removed by etching in a 0.5 M $FeCl_3$ aqueous solution. The graphene/polymer film is rinsed in DI water and then transferred to SiO_2(300 nm)/Si substrate. The polymer support is subsequently removed by immersion in acetone followed by rinsing in IPA and drying under a N_2 flow.

Exposure of graphene/oxide to ozone was carried out in the Cambridge Nanotech Savannah System (S100 G1). A series of ozone pulses were performed over one minute each with a dose of ∼40 mbar s and N_2 purge of 1 s between pulses.

Optical microscopy and Raman spectroscopy (Renishaw Raman InVia microscope, 632 nm wavelength with 1 mW delivered to the sample, 50x objective) are performed after graphene is transferred to SiO_2(300 nm)/Si substrates.

Results

Figure 1(a) schematically outlines our etching-free transfer process using ALD alumina as support layer. The first step is the ALD of alumina directly onto CVD graphene-covered Cu catalyst foil (more details in supporting information) under continuous-flow mode without a seed layer [41]. As

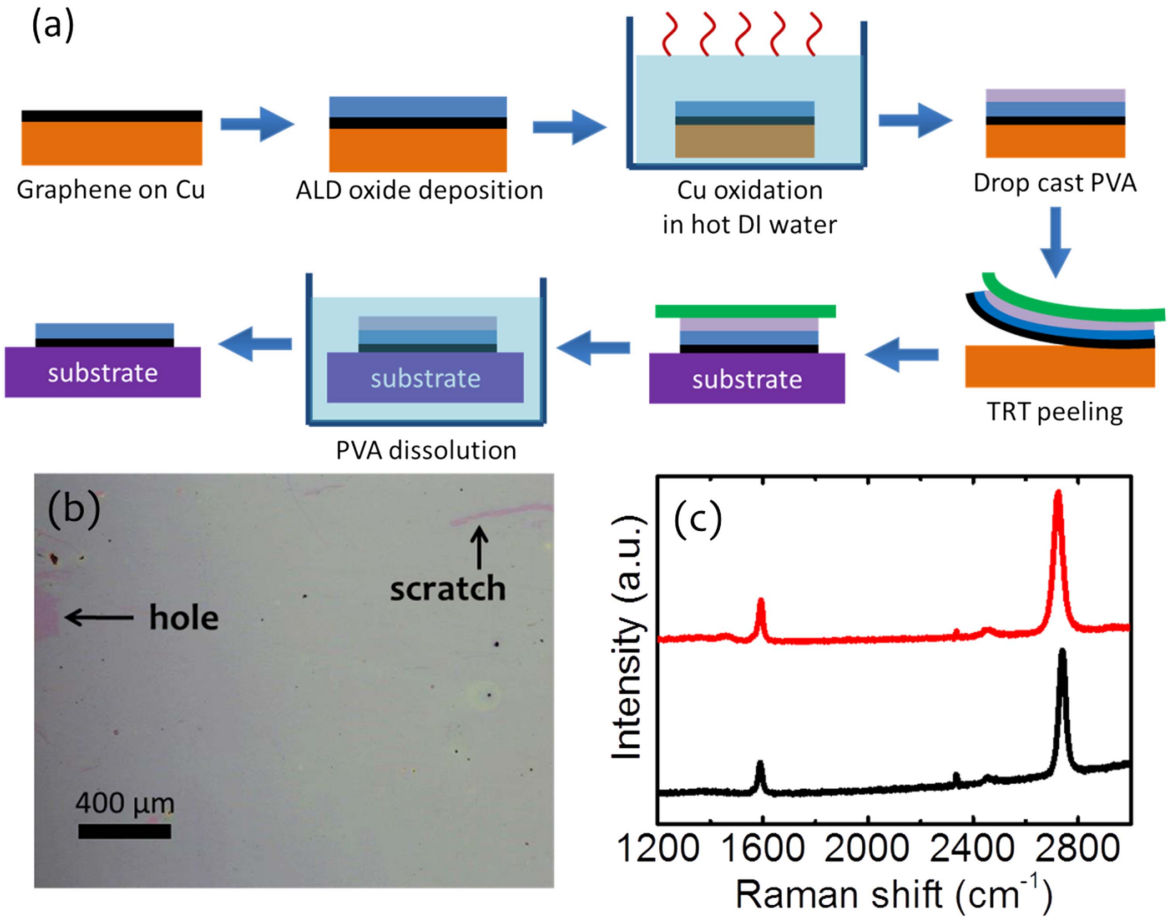

Figure 1. (a) Schematic representation of the transfer process with oxide buffer layer between graphene and polymer. (b) Optical micrograph of graphene transferred to SiO_2(300 nm)/Si using the process shown in (a). (c) Raman spectra of as-grown graphene on Cu foil –black line– and of graphene transferred to SiO_2(300 nm)/Si using the process shown in (a) –red line–.

confirmed by spectroscopic ellipsometry, a 40 nm ALD oxide thickness was used here, noting that the oxide thickness can be adapted to a chosen application, for example to achieve a certain gate oxide thickness in top-gated transistors. The sample is then immersed in DI water at ~50 °C for ~12 h to oxidize the Cu foil. The creation of Cu oxide decouples the graphene from the catalyst [49–51] making it easier to peel from the Cu foil. A poly(vinyl) alcohol (PVA) solution (2 g in 20 ml DI water) is drop-cast on top of the alumina layer and heated to 70 °C for 10 min [52] to provide additional mechanical support for the graphene/alumina film. The sample is removed from the hot plate and a thermal release tape (TRT) (Nitto Denko) is placed on top of it. The Cu foil is then peeled off and the TRT-PVA-alumina-graphene layer stack is transferred onto a SiO_2(300 nm)/Si support for the fabrication of field effect transistors (FETs). We acknowledge that the formation of wrinkles, cracks and holes can occur as a result of this process, as highlighted in figure 1(b). After the transfer, the substrate is heated to 120 °C to ensure the release of the TRT. The sample is then immersed in warm DI water (50 °C) for at least 1 h to dissolve the PVA and finally dried with N_2. We highlight that although Cu foils are used here, the use of oxides to support graphene transfer is a method applicable to graphene grown on other CVD metal catalysts where other treatments can be used to weaken the graphene–catalyst interaction.

We use optical microscopy and Raman spectroscopy for the initial characterisation of as-transferred graphene. Figure 1(b) shows an optical image of the transferred graphene/alumina bilayer, where the contrast with the SiO_2(300 nm)/Si support is highlighted by a hole and a scratch in the film. Figure 1(c) compares the Raman spectrum of as-grown CVD graphene on Cu foil (black line) with graphene transferred onto SiO_2(300 nm)/Si with 40 nm of alumina (red line) using the process described in figure 1(a). Both samples show the characteristic features of single layer graphene (2D FWHM $<40\ cm^{-1}$ and $I_{2D}/I_G > 2$) whilst the negligible D peak confirms high graphitic quality and negligible defects and disorders introduced by this transfer process. As-grown graphene on Cu shows a 2D peak fitted with a single Lorentzian with FWHM = 36.9, $I_{2D}/I_G = 3.4$ and the G and 2D peak positions at 1590 cm^{-1} and 2740 cm^{-1}, respectively. Raman spectra collected on graphene after transfer shows a 2D peak fitted with a single Lorentzian with FWHM = 38.5, $I_{2D}/I_G = 3.1$ and the G and 2D peak positions at 1593 cm^{-1} and 2723 cm^{-1}, respectively.

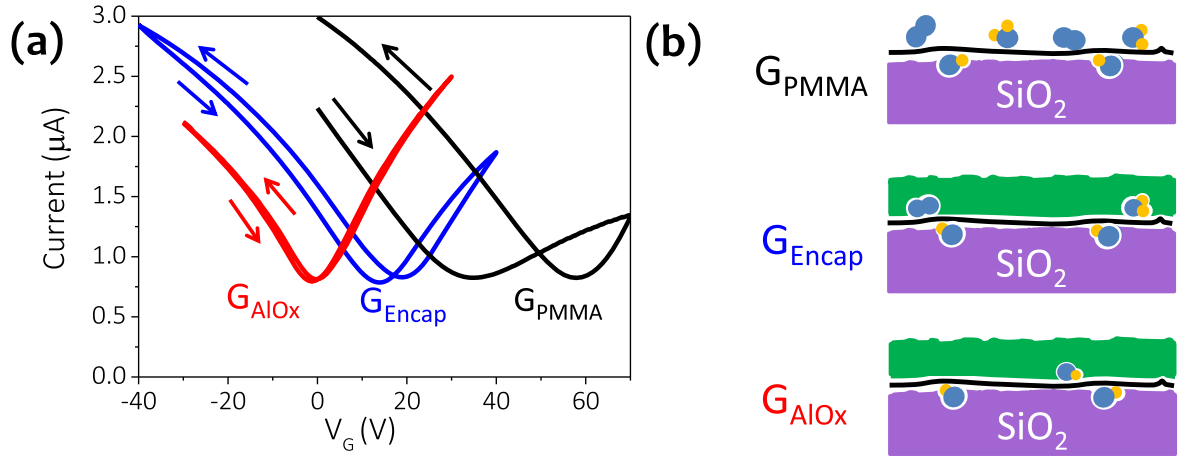

Figure 2. (a) Transfer characteristics of back-gated two terminal transistors fabricated with three different processing approaches, as described in the main text. Source–drain bias was $V_{SD} = 10$ mV. (b) Schematic representation of graphene/metal-oxide/SiO_2 interface of various devices measured in (a).

One of the most common graphene device architectures, that serves as a building block for a number of graphene applications, is the FET. There are a number of key metrics which may be used to define FET device performance. Whilst particular effort has been focussed on improving the field-effect mobility [39, 53, 54], real-world applications have stringent requirements on stable and consistent operation. As such, additional factors including gate-induced hysteresis and unintentional doping are crucial parameters to be minimised for graphene applications. Back-gated (300 nm SiO_2 on doped-Si) graphene FET devices were fabricated using photolithography (see Methods and supporting information) to further characterise the graphene. All electrical measurements were carried out in ambient conditions at room temperature. We use three different processing approaches to fabricate graphene-based FETs (as described further in the supporting information): (1) transfer with PMMA support layer [G_{PMMA}], (2) transfer with PMMA followed by the post-transfer deposition of 40 nm ALD alumina [G_{Encap}] and (3) depositing 40 nm alumina as protective layer prior to transfer using the method outlined in figure 1(a) [G_{AlO_x}]. For the latter approach the alumina was selectively etched in diluted phosphoric acid to allow contact metallisation whilst leaving the graphene channel protected, as described in the supporting information.

By measuring the Dirac point V_D, i.e. the gate voltage at which minimum current is observed, and the change in V_D between the up sweep (negative to positive) and the down sweep (positive to negative) ΔV_D, we can extract the interface charge trap density $\Delta n = C_g \Delta V_D / e$, as well as the residual carrier density (calculated for the up sweep) $n_{res} = C_g V_D / e$, where the gate capacitance $C_g = 11.6\,\mathrm{nF\,cm^{-2}}$, and e is the electronic charge. Figure 2(a) shows the field-effect transport characteristics of devices fabricated via the three different graphene processing approaches. The G_{PMMA} FET shows high p-type doping ($n_{res} > 2 \times 10^{12}\,\mathrm{cm^{-2}}$) and a large hysteresis between the up and the down sweeps ($\Delta n > 1.6 \times 10^{12}\,\mathrm{cm^{-2}}$) which is typical for unencapsulated graphene on SiO_2 transferred with PMMA. A significant but incomplete reduction in hysteresis and doping can be obtained for G_{Encap}, which is consistent with previous reports after the direct deposition of ALD alumina on polymer transferred graphene [55]. Further improvements can be obtained using thicker encapsulating films as well as optimised seed layers [38]. The long term encapsulation of graphene transistors has also been demonstrated using *in situ* gaseous pretreatments where conformal growth of oxide passivates charge traps on the graphene surface [39]. However, these methods use graphene after transfer with PMMA and thus, are prone to the degradation it involves. Ultimately during the initial exposure to PMMA during transfer some adsorbates will remain trapped between the graphene and alumina layer after encapsulation causing a finite level of doping and hysteresis, as schematically shown in figure 2(b).

Table 1. Comparison of the charge trap density Δn, and residual carrier density n_{res} (determined from the up sweep) extracted from the plots in figure 2 and compared to values in the literature.

Graphene process	$\Delta n \times 10^{10}$ ($\mathrm{cm^{-2}}$)	$n_{res} \times 10^{10}$ ($\mathrm{cm^{-2}}$)
G_{PMMA}	165	254
G_{Encap}	37	102
G_{AlO_x}	6	7
30 nm ALD Al_2O_3 [55]	86	Not given
90 nm ALD Al_2O_3—Oxidised Al seed layer [38]	0–17	11.5
90 nm ALD Al_2O_3—H_2O pretreatment [39]	6	14.5

The $I_D - V_G$ behaviour of G_{AlO_x} (figure 2(a)) shows negligible doping ($n_{res} < 1 \times 10^{11}\,\mathrm{cm^{-2}}$) and very low hysteresis ($\Delta n < 1 \times 10^{11}\,\mathrm{cm^{-2}}$) compared to G_{Encap}. Given that the same ALD growth conditions were used for each process, the clear improvement between G_{Encap} and G_{AlO_x} can thus be predominantly attributed to the significant reduction in the number of processing-induced adsorbents at the interface between graphene and alumina, as schematically shown in figure 2(b). Table 1 compares the FET device metrics for

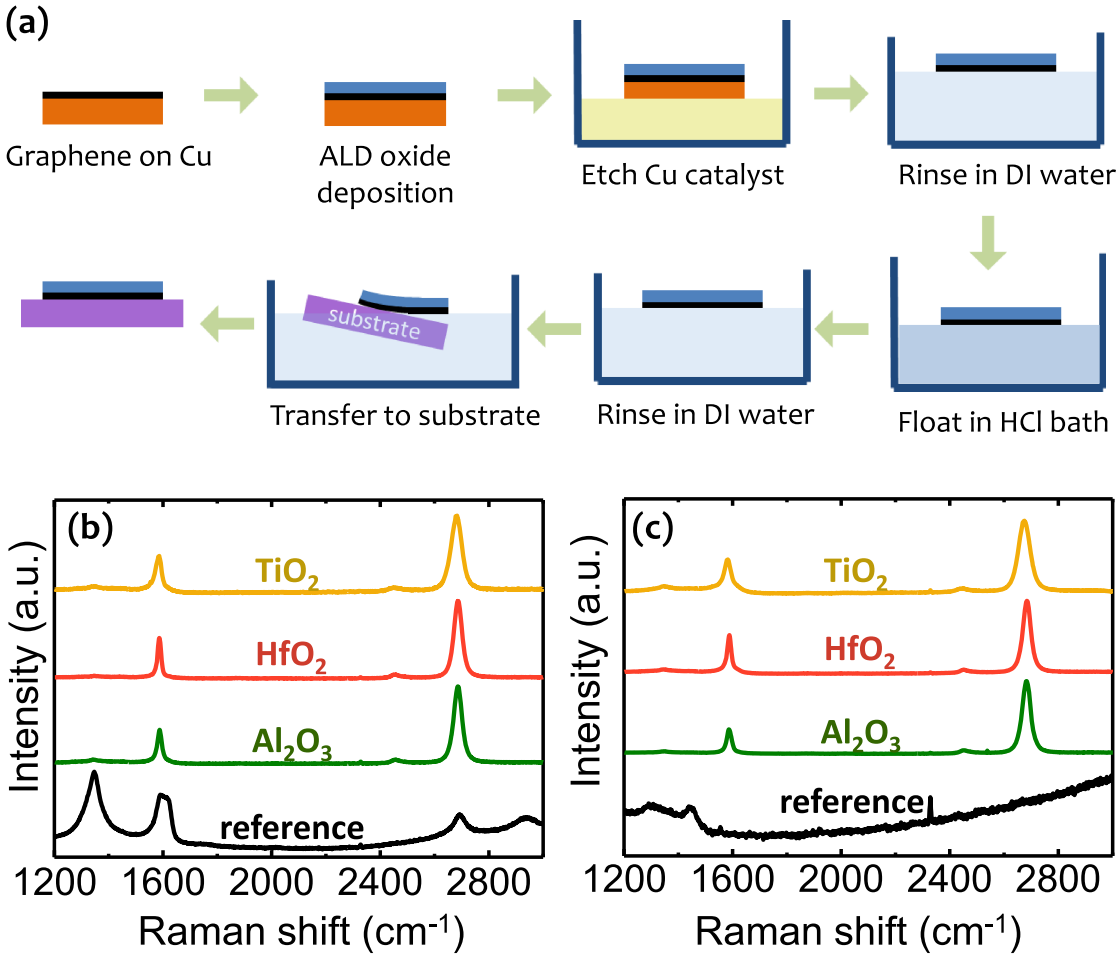

Figure 3. (a) Schematic representation of the second oxide transfer process where polymer is completely avoided. Comparison of Raman spectra of graphene transferred with metal oxide layers and G_{PMMA} as reference after exposing to harsh gas environments: (b) ozone treatment for 1 min at 200 °C, which is comprised of a series of ozone pulses each with a dose of ~40 mbar s and N_2 purge between pulses of 1 s in the same system used for ALD and (c) oxygen plasma for 1 min at 100 W and 150 mbar.

the three different processes, which for G_{AlO_x} devices are comparable with some of the lowest hysteresis values for graphene FETs in the literature [38, 39]. This highlights the benefits of the proof-of-concept oxide transfer technique demonstrated here, that avoids any direct contact of the graphene with polymers or etchants.

The use of polymers during the transfer process can be completely avoided by depositing a thicker layer of ALD metal oxide. Figure 3(a) shows the steps followed for this transfer method. 100 nm of either alumina, hafnia or titania are directly deposited onto graphene on Cu foil under continuous-flow mode without using a seed layer [41]. The thickness was determined to give enough support to the graphene during the transfer process which simultaneously provides more stability to graphene devices due to its encapsulation [38]. Cu foil is then etched using a 0.5 M $FeCl_3$ aqueous solution (~12 h) for a sample size of 1 × 1 cm^2 and transferred to DI water. Samples are then floated in HCl 37% for 15 min to remove any residual Fe ions left from the etchant [56]. A second DI water bath is used to rinse the samples and they are finally removed from the water onto a SiO_2(300 nm)/Si substrate.

Additional tests were carried out to confirm the robustness of the film transferred with the metal oxides. Three samples of SLG were transferred each with a 100 nm thick layer titania, hafnia and alumina, respectively, following the process outlined in figure 3(a). Samples of graphene transferred with each of the metal oxides were heated to 200 °C and exposed to ozone for 1 min (see methods for more details). Furthermore, different samples of graphene transferred with the three metal oxides were exposed to oxygen plasma (1 min, 100 W, 150 mbar) at room temperature. Reference samples of SLG transferred with conventional processes using PMMA and not protected with a metal oxide layer were also exposed to ozone and oxygen plasma at the same time.

Raman spectra taken from the top of the samples after oxygen plasma and ozone treatments are shown in figures 3(b) and (c). The annealing of unprotected graphene under an oxidizing atmosphere such as ozone leads to degradation as shown for the unprotected reference sample in figure 3(b) (black line). Similarly, the conditions used for the oxygen plasma are expected to completely remove unprotected graphene, since a shorter (8 s) and lower power (50 W)

oxygen plasma treatment performed at the same pressure on a sample without any metal oxide layer leads to the complete absence of a 2D peak in the Raman spectra, as observed in figure 3(c) (black line). The samples transferred with the oxide support layers show no significant increase in the measured D-peak of the Raman spectra after the ozone and oxygen plasma treatments. This confirms the oxide support layer effectively protects the SLG from harsh oxidising environments maintaining the quality of the graphene.

Discussion

While ALD of metal oxides has been widely used for graphene FETs, here we demonstrate a more integrated approach to device fabrication, where the same ALD layer can serve as graphene protection, support, encapsulation and functional device layer. Our data showed that a 40 nm ALD alumina layer directly deposited on the graphene/catalyst after the growth enables a significant reduction in the number of processing-induced adsorbents during FET fabrication and hence significantly reduced charge trap and residual carrier densities. Our method aides integrated device manufacturing, effectively eliminating an additional step. While ALD films offer graphene protection, selective etching of the oxide is required to contact the graphene for typical device structures. The selective etching of oxide films has been well studied and multiple methods have been reported including wet [57, 58] (e.g. KOH, HF, piranha) and dry [59–62] (e.g. RIE, ICP, DRIE) processes. However, we found that etching of the metal-oxide layer here was not straight forward which may relate in part to the growth mechanisms of ALD oxides on graphene [41]. Extensive process calibration was required to avoid leaving oxide residues or damaging the graphene. Although we note that complete etching of the graphene might be beneficial in the contact area to lower contact resistance by producing edge contacts (side contact instead of top contact) [63–65].

Our method here relies on the transfer and processing of graphene/ALD bilayer structures. ALD oxide growth is conformal and thus, is prone to 'freeze in' graphene wrinkles on the catalyst surface (see atomic force microscopy in supporting information) which can be detrimental to the transport properties. The transfer process can also introduce strain in the graphene and damage the oxide and graphene films. The transfer process involves handling and bending of the oxide/graphene film which can induce cracks that may lead to significant reduction of film quality. The thinner the oxide layer the more flexible it is, and according to literature 40 nm films of ALD deposited alumina start showing cracks at a bending radius of 14 mm [66]. To partly address these challenges, our method can be modified into a two-stage process where following the initial transfer with a thin ALD layer an additional layer of oxide is deposited.

We have so far considered the ALD oxide/graphene interface, however, the substrate interface is equally important for device performance. We focus here on SiO_2 as the most widely used support, yet it is well known that the measured graphene mobility is limited by its interaction with this substrate [67, 68]. This can be addressed via alternative support (such as h-BN) [67], or partly by plasma treatments and reoxidation of the SiO_2 substrate [69]. Furthermore, we have shown that during oxide ALD, H_2O/O_2 redox couples and the presence of silanol groups at the graphene—SiO_2 interface can cause doping and hysteretic behaviour [30, 38, 70]. So apart from just avoiding substrate contamination, it is also important to ensure the integrity of the relevant device interfaces during the entire process flow.

Herein, we focus on FET model devices, but this integrated approach may be interesting for a wide range of graphene applications where scalability and reliable device performance are critical challenges. For dye-sensitized solar cells [71–73], for instance, using ALD titania as the support layer would provide a clean interface between the graphene and the titania whilst the titania can also serve as a compact layer to reduce charge recombination losses [74]. It is conceivable that dopant materials could be incorporated at the graphene-oxide interface to strongly dope the graphene for applications requiring low sheet resistance such as organic light emitting diodes [75]. The oxide support may also be exploited as a hard mask [76] in devices avoiding the use of polymers and other organic solvents that can leave undesirable carbon residues on the graphene surface.

Conclusions

We have demonstrated the concept of using ALD oxide films not only for graphene interfacing and post-growth encapsulation but also as a protective and supporting layer for CVD graphene transfer and integrated FET fabrication. Back-gated graphene FET devices transferred with ALD alumina show significantly reduced charge trap and residual carrier densities. Our method avoids any direct contact of the graphene with polymers and through the use of thicker ALD layers ($\geqslant$100 nm), polymers can be eliminated from the transfer-process altogether. The ALD film can be kept as a functional device layer, facilitating integrated device manufacture. Many of the challenges for 2D materials are essentially linked to interfacing with non-2D materials and we think the combination of CVD and ALD thereby offers many opportunities that underline the wider relevance of our data here.

Acknowledgments

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